Getting Started with Circuit Design: Transmission Line, Mixer, and Channel

ANSYS, Inc.
Southpointe
2600 Ansys Drive
Canonsburg, PA 15317
ansysinfo@ansys.com
https://www.ansys.com
(T) 724-746-3304
(F) 724-514-9494

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Conventions Used in this Guide

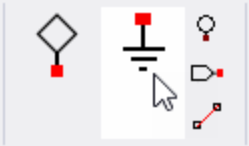
Please take a moment to review how instructions and other useful information are presented in this documentation.

- Procedures are presented as numbered lists. A single bullet indicates that the procedure has only one step.
- Bold type is used in the following circumstances:
  - Keyboard entries that should be typed in their entirety exactly as shown. For example, "**copy file1** " means you must type the word **copy**, then type a space, then type **file1**.
  - On-screen prompts and messages, names of options and text fields, and menu commands. Menu commands are often separated by greater than signs (>). For example, "click **HFSS** > **Excitations** > **Assign** > **Wave Port**."
  - Labeled keys on the computer keyboard. For example, "Press **Enter** " means to press the key labeled **Enter**.
- Italic type is used in the following circumstances:
  - Emphasis.
  - The titles of publications.
  - Keyboard entries when a name or a variable must be typed in place of the words in italics. For example, "**copy***filename***"** means you must type the word **copy**, then type a space, then type the name of the file.
- The plus sign (+) is used between keyboard keys to indicate that you should press the keys at the same time. For example, "Press **Shift**+**F1**" means to press the **Shift** key and, while holding it down, press the **F1** key also. You should always depress the modifier key or keys first (e.g., **Shift**, **Ctrl**, **Alt**, or **Ctrl**+**Shift**), continue to hold it/them down, then press the last key in the instruction.

Accessing Commands: *Ribbons, menu bars,* and *shortcut menus* are three methods that can be used to see what commands are available in the application.

- The *Ribbon* occupies the rectangular area at the top of the application window and contains multiple tabs. Each tab has relevant commands that are organized, grouped, and labeled. An example of a typical user interaction is as follows:

  "Click **Schematic** > **Ground** "



This instruction means that you should click the **Ground** command on the **Schematic** ribbon tab. An image of the command icon, or a partial view of the ribbon, is often included with the instruction.

- The *menu bar* (located above the ribbon) is a group of the main commands of an application arranged by category such File, Edit, View, Project, etc. An example of a typical user interaction is as follows:

  "From the **File** menu, select the **Open Examples** command" means click the **File** menu, then click **Open Examples** to open an explorer window to the **Examples** folder.

- Another alternative is to use the *shortcut menu* that appears when you right-click. An example of a typical user interaction is as follows:

  “Right-click and select **Assign Excitation** > **Wave Port**" means select an object, right-click, and click an option on the shortcut menu that appears.

Getting Help: Ansys Technical Support

For information about Ansys Technical Support, go to the Ansys corporate Support website, http://www.ansys.com/Support. You can also contact your Ansys account manager in order to obtain this information.

All Ansys software files are ASCII text and can be sent conveniently by e-mail. When reporting difficulties, it is extremely helpful to include very specific information about what steps are taken or what stages the simulation reached, including software files as applicable. This allows more rapid and effective debugging.

Help Menu

To access help on the Help menu, select **Help**. Then choose one of the following options:

- **[product name] Help** - opens the contents of the help. This help includes the help for the product and its *Getting Started Guides*.
- **[product name] Scripting Help** - opens the contents of the *Scripting Guide*.
- **[product name] Getting Started Guides** - opens a topic that contains links to Getting Started Guides in the help system.

Context-Sensitive Help

To access help on the user interface, press **F1** to open the help topic specific to the active product (design type).

You can press **F1** while the cursor is pointing at a menu command or while a particular window or tab is open. In this case, the help page associated with the command or open window is displayed automatically.

Table of Contents

1 - Getting Started with Circuit Design

Getting Started with Circuit Design provides step-by-step instructions on how to get started with the **Circuit Design** type of the Ansys Electronics Desktop. Learn how to start Ansys Electronics Desktop, build basic designs, analyze the designs and generate reports showing the performance of those designs. Learn with the help of examples how to set up each of the design types, start the simulation, and perform post-processing in the following chapters.

- Introduction
- Basic Transmission Line
- Simple Mixer
- Simple Channel
- Low Pass Filter

Note: The next chapter, Circuit Design Overview, outlines the basic steps for using **Electronics Desktop**. If you want to skip the overview and just start the tutorials, go to Chapters 3, 4, and 5 on setting up and solving a transmission line, mixer, and channel.

2 - Circuit Design Overview

This chapter briefly introduces the basic steps for setting up and running a design project in the **Electronics Desktop** (**Electronics Desktop**). The focus is on circuit and system analysis and the framework required to design RF-microwave, signal integrity, and printed circuit board applications. The initial steps are 1.) launch **Electronics Desktop**, 2.) start a new project, and 3.) enable the **Choose Technology** window (optional).

Launch Electronics Desktop

To launch **Electronics Desktop**, click the **Electronics Desktop** shortcut icon:

Start a New Project

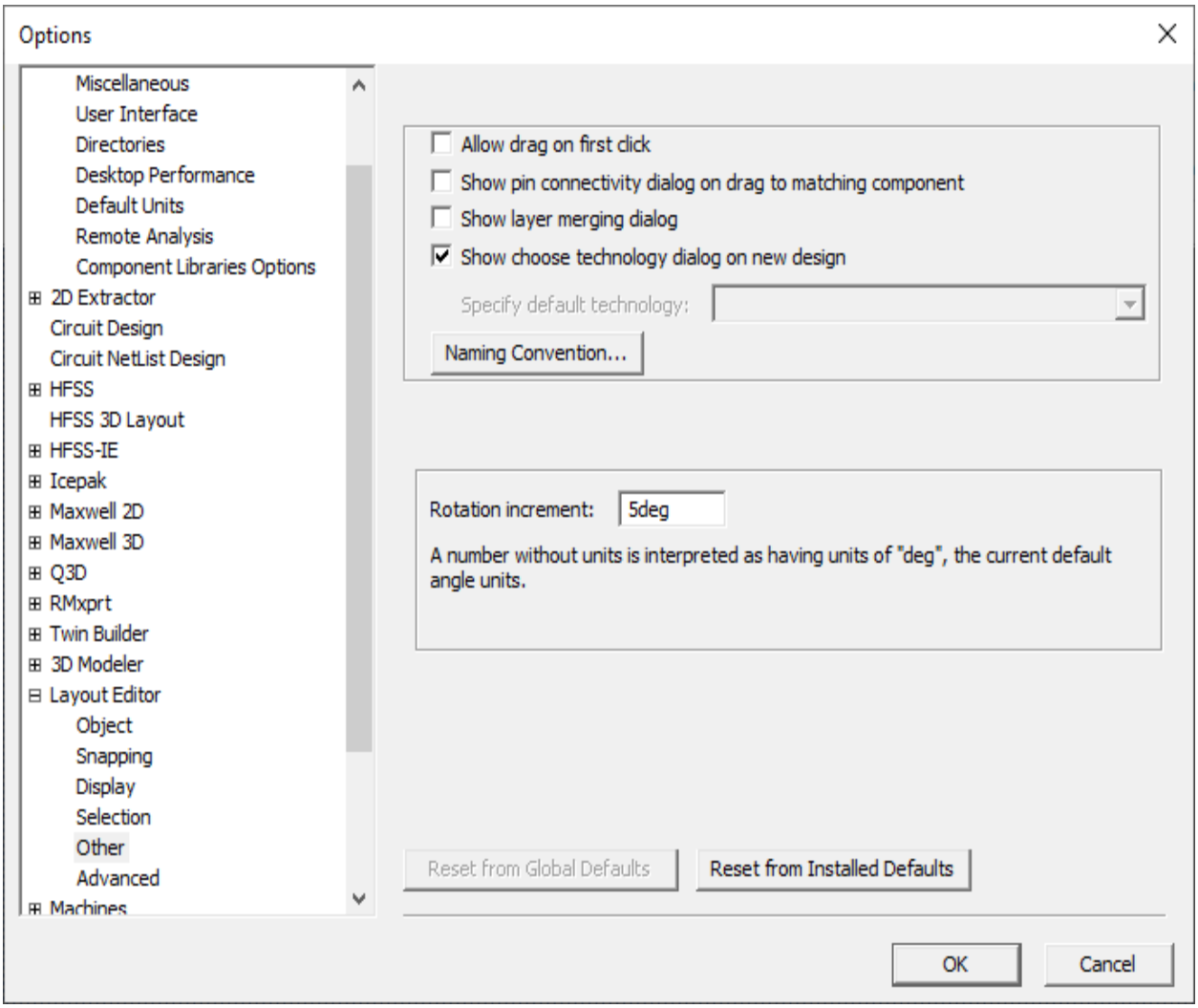
When you launch **Electronics Desktop**, a new project may be created for you (Project 3 in the example above). If a new project is not automatically created, go to the **File** menu and click **New** to start one. A project can contain one or more designs.

Enable Technology Dialog

If your Circuit design uses a field solver, you may need to select the layout technology before opening the design. Complete the following steps to ensure that the appropriate window opens.

1. Go to **Tools** > **Options** > **General Options**.
2. From the **Options** window, expand the **Layout Editor** and select **Other**.
3. Ensure the **Show choose technology window on new design** option is selected and

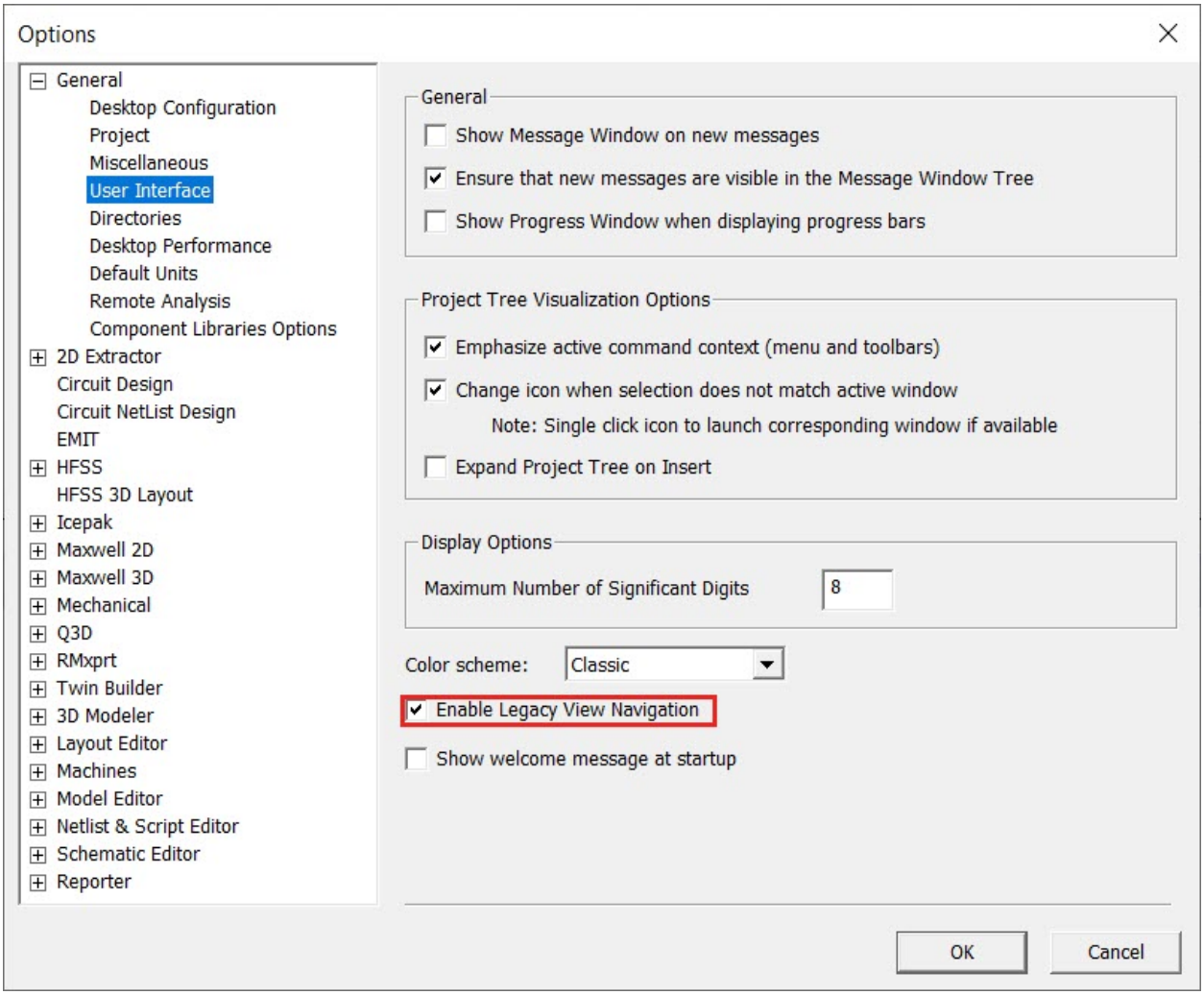
click **OK**.



Enable Legacy View

To view orientations consistent with the instructions and images in the guide, enable legacy view navigation.

1. Go to **Tools** > **Options** > **General Options**.
2. From the **Options** window, expand **General** and select **User Interface**.
3. Check **Enable Legacy View Navigation**



The subsequent workflow involves these steps:

- Select the type of design to create.
- Define the initial physical stackup, if required.
- Populate the design with components and layout objects.
- Add ports and/or sources.
- Create a solution setup.
- Analyze the design.
- Generate an analysis report.

Related Topics

Select Design Type

Select Design Type

The framework for **Electronics Desktop** depends upon the design type that you insert for creating your design. After launching Ansys Electronics Desktop, start a new project and select the appropriate design type. Either select the design type from one of the options that appear under the **Project** menu or click one of the **Insert** options on the toolbar.

Some of the supported design types include:

- **Insert Circuit Design** — A schematic-based interface to the circuit simulator.
- **Insert Circuit Netlist** — A netlist (text-based) interface to the circuit simulator.
- **Insert 2D Extractor Design** — A 2D solver for extracting per-unit-length RLGC parameters of transmission lines.

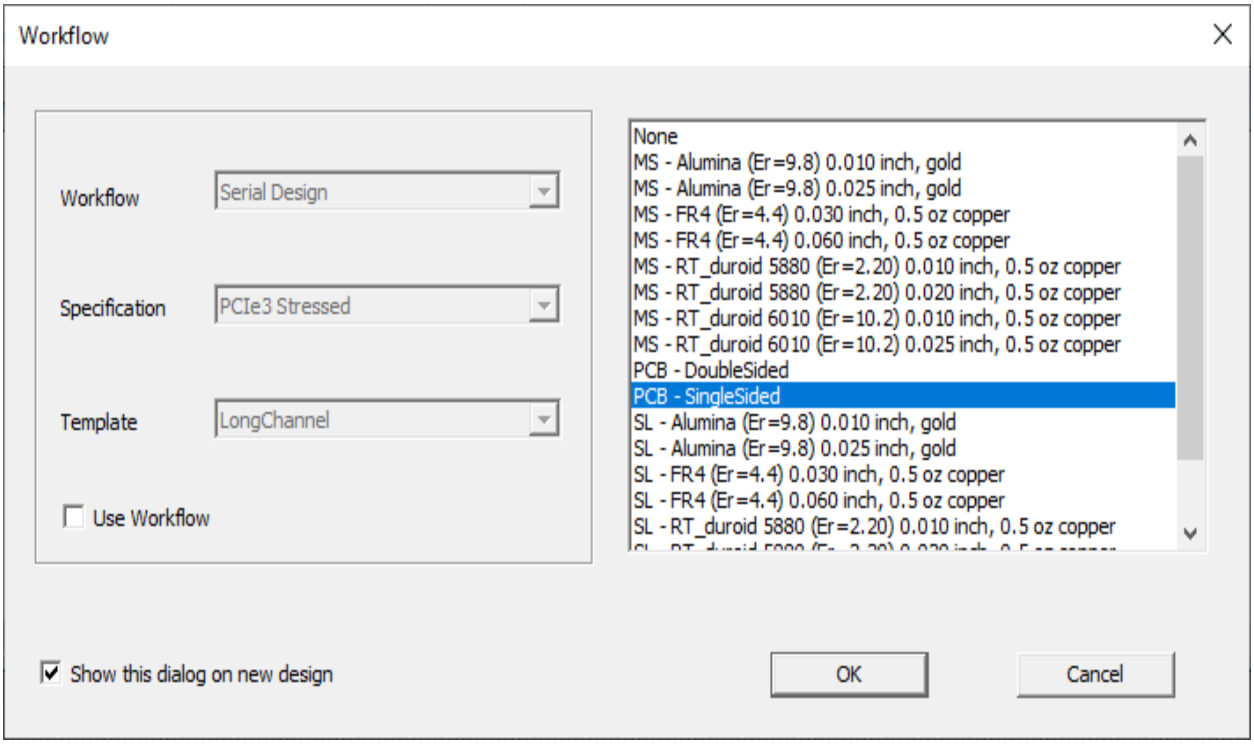
This document describes the overall framework when ANSYS Electronics Desktop is used as a circuit- and system-based simulation when you **Insert Circuit Design**.

When you create a new design, Ansys Electronics Desktop stores the data in a *project* file. Project files in **Electronics Desktop** have an “*.aedt" extension on your hard drive. A single project file can contain many different designs and design-types.

The next step is to define the initial physical stackup.

Define the Initial Physical Stackup

When you open a Circuit design, the **Workflow** window opens (if the option has been enabled as described earlier).



The **Workflow** window also lets you define the initial physical stackup for your design.

Technology files contain groups of standard, preset traces, and substrates that define the physical stackup of a design. Several standard technology files are included in the **Electronics Desktop**. When you start a new design:

- use an existing technology file.
- create your own custom technology file.
- import an .xml file.
- start with a preset technology file , then modify the stackup. (this can be done any point in your design process.)
- choose not to use a preset technology file by clicking **None**.

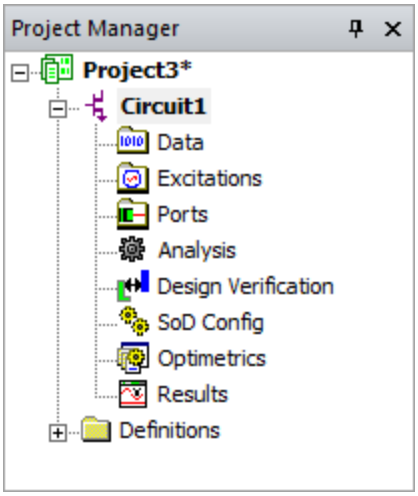
The set of standard technology files included are primarily for RF-microwave and printed circuit board applications.

> **Note:** HFSS 3D Layout and planar EM designs require a physical stackup or technology file. Circuit designs using only ideal components do not require a stackup. The **Circuit Netlist** type likewise does not need a physical stackup.

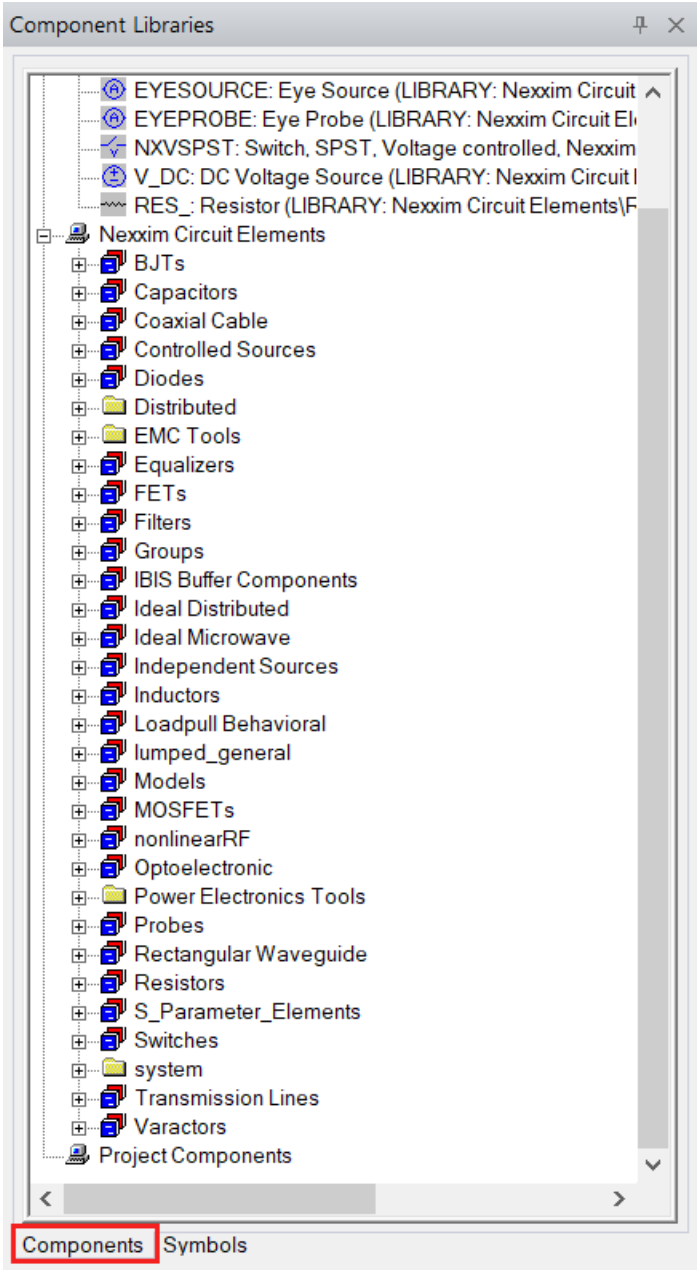
The next step is to populate the design.

Populate the Design

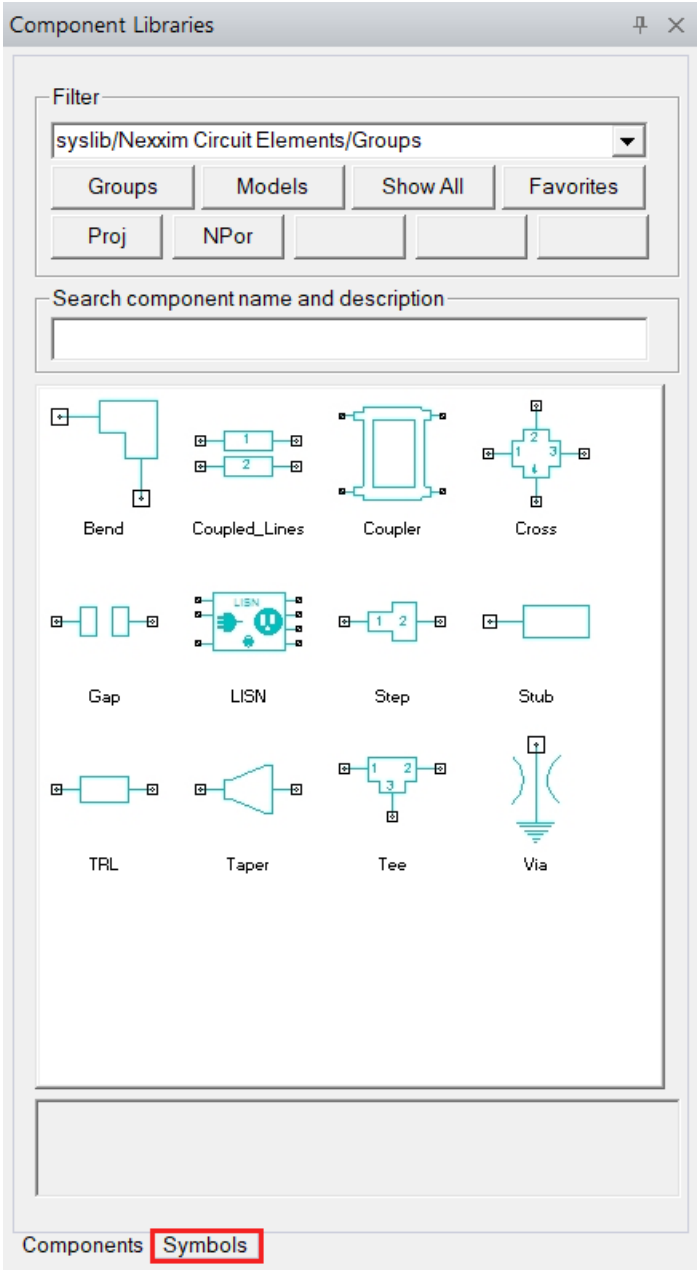
If you select **Insert Circuit Design** on the **Project** menu, the **Project Manager** window is populated with the **Circuit Design** type as shown in the following figure.



Circuit components are found in the **Component Libraries** window. In its **Components** tab, expand groups of components, then drag components onto the schematic.



From the **Symbols** tab, use the **Search** field to find components by keywords. To create your design, add components to your schematic and/or add geometry to your layout. Include linked (HFSS, Q3D, SIwave, etc.) and imported models (measured data) as appropriate.



Some useful operations to work with components are:

- Press **R** on your keyboard to rotate a component before it is placed. Press **Esc** or right-click and use the shortcut menu to finish placing the component.
- Once several components are placed on the schematic, wire them together by dragging them closer together so their pins touch. Even if the components are dragged apart, they remain wired. Or use the **Wire** command under the **Draw** menu or the wire icon on the toolbar. If appropriate, add a ground using the toolbar icon.

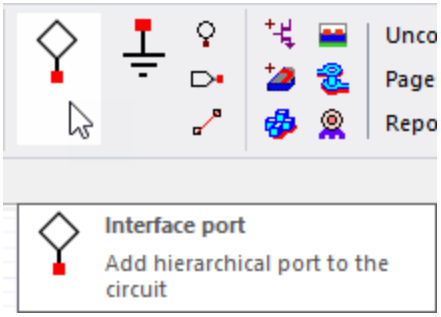
- The schematic can be centered by pressing **Ctrl-D**. Pan the schematic by clicking and dragging, while holding **Shift**. Zoom the schematic in and out by holding **Shift** +**Alt** while clicking and dragging.

The next step is to add ports and sources.

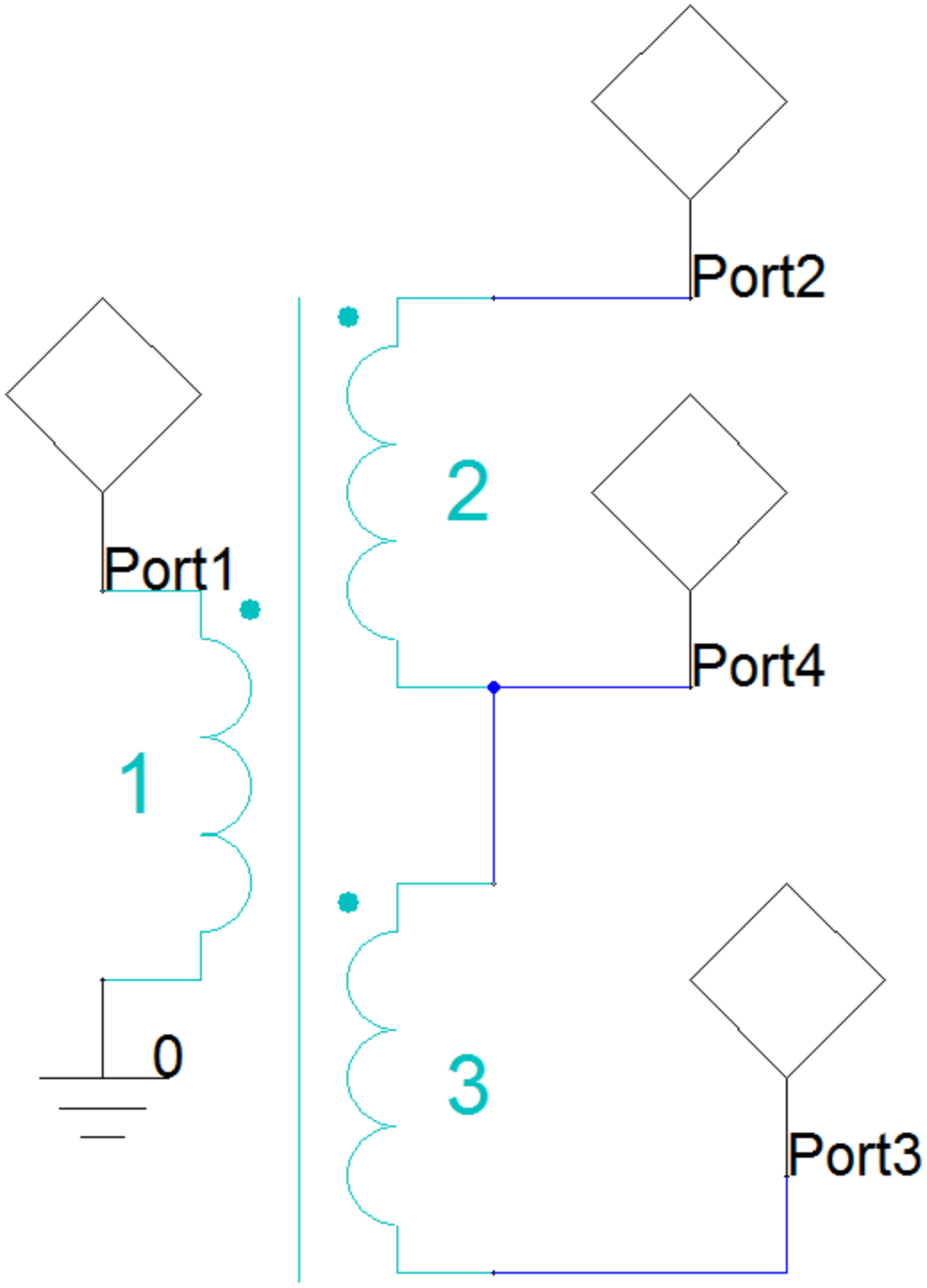
Add Ports in a Circuit Design

The type of ports and sources you add depends on the type of design you want to analyze and the type of analysis you want to run. For example, in circuit designs, usually ports are added to the schematic that include default terminations, while sources can be added independently to a circuit or configured/included within a port.

The simplest way to add a port to a circuit is to select the **Interface Port** icon on the toolbar , then place the port into your schematic.



> **Note:** The interface port option also appears under the menu item **Draw** > **Interface Port**.

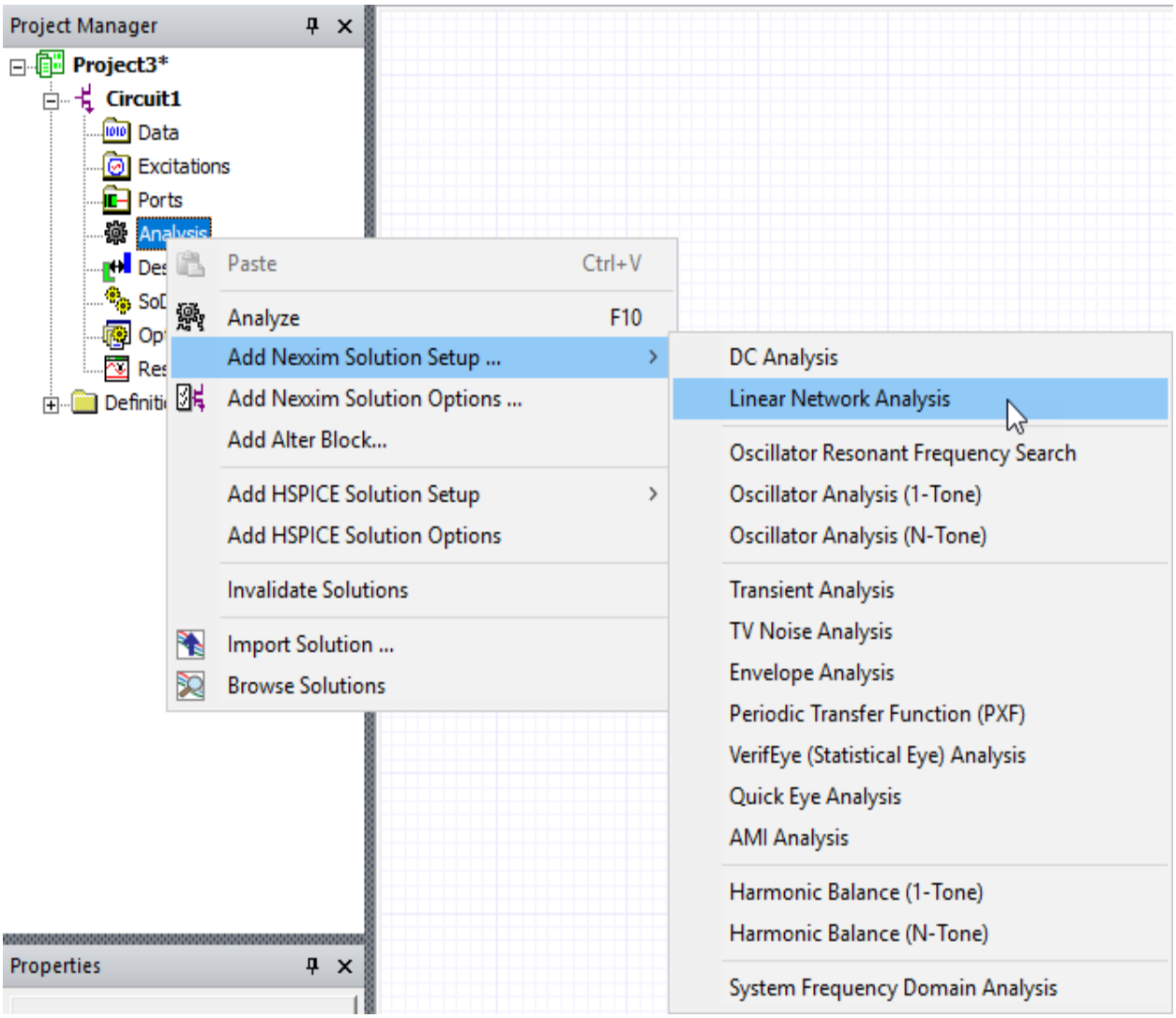


The next step is to create a solution setup.

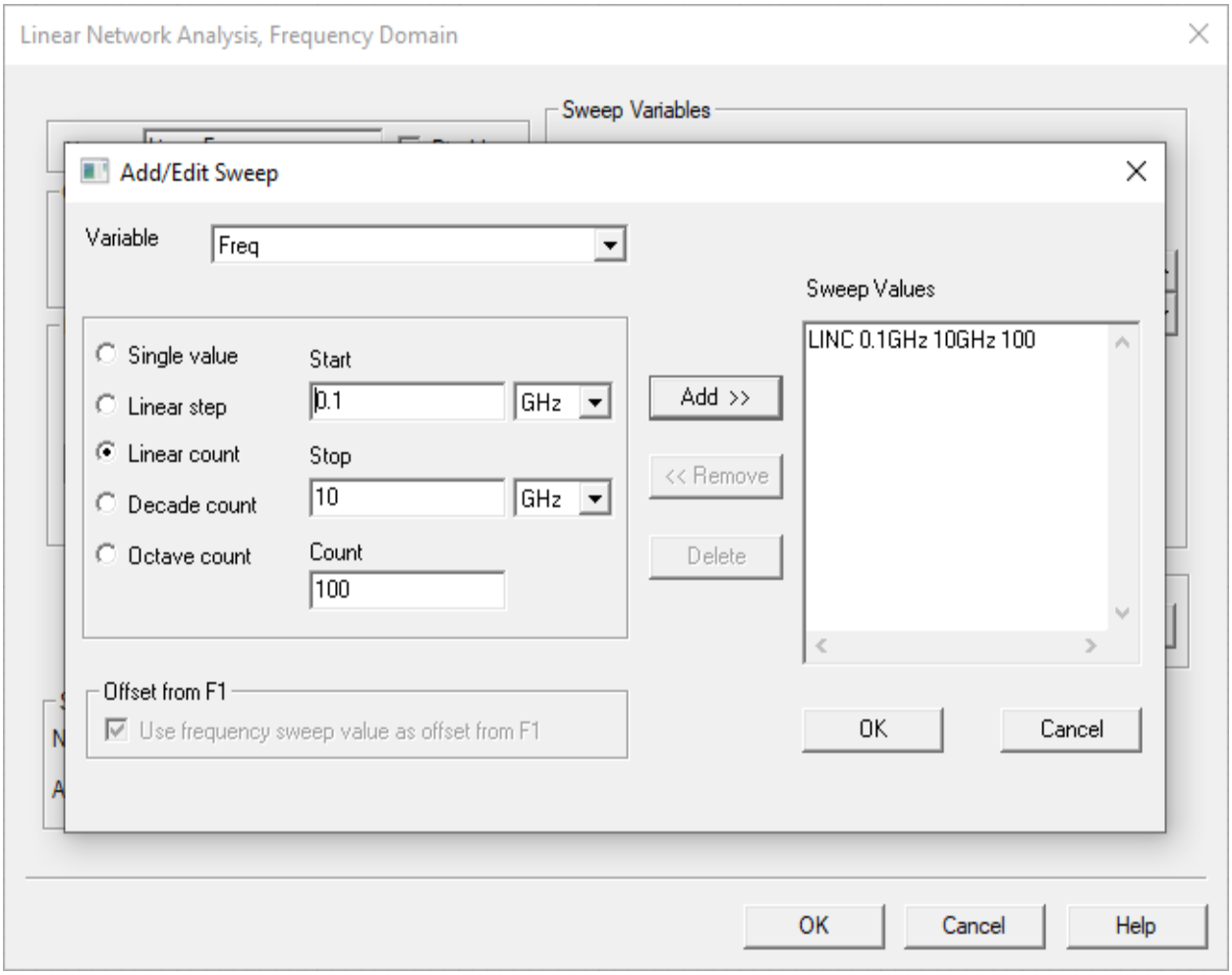
Create a Solution

Create a solution setup to specify which type of analysis to perform and the frequencies and time ranges to analyze. For a circuit design, add frequency sweeps, transient analyses, harmonic-balance analyses, and several other types of setups.

To add a solution setup to a circuit design, on the **Project Manager** window, right-click **Analysis** and select **Add Nexxim Solution Setup**, then select the appropriate analysis type.



A window opens to let you add a frequency or parameter sweep if appropriate. For example, to add a frequency sweep using a **Linear Network Analysis** setup window, as shown in the following figure, click **Add** and set the frequency values.

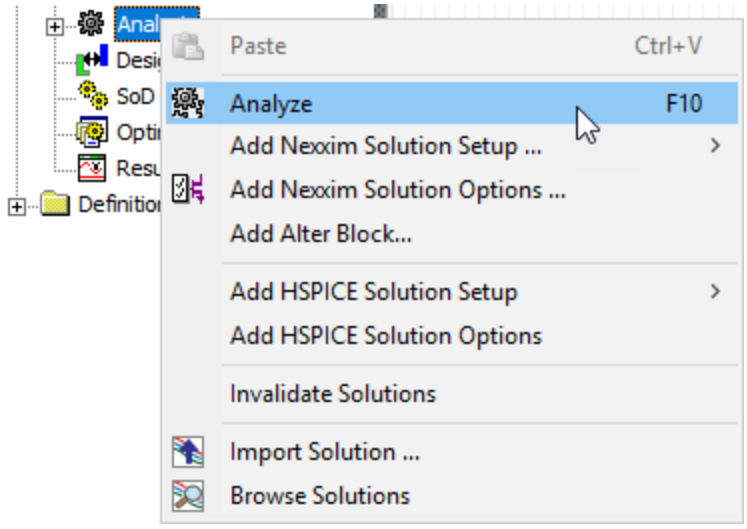


When you have finished configuring the setup, click the **OK** buttons to close each open window.

The next step is to analyze the design.

Analyze the Design

From the **Project Manager** window, expand the **Project Tree** and [*active design folder*]. Then right-click **Analysis** and select **Analyze**.

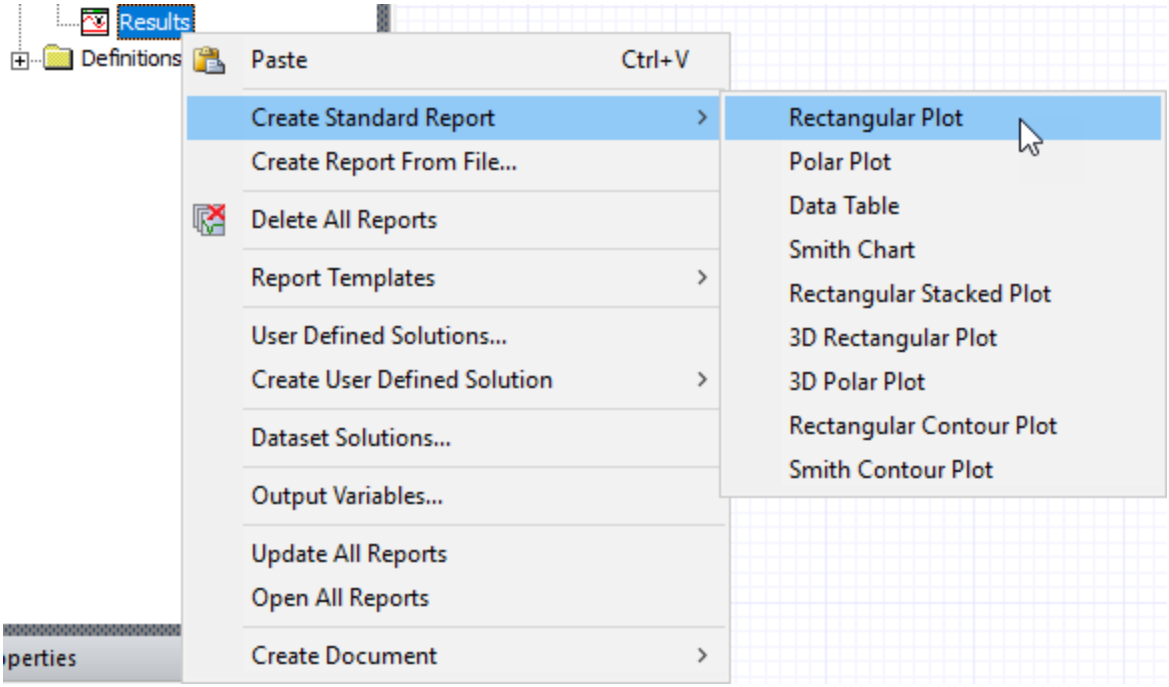


Ansys Electronics Desktop displays a progress bar on the screen and periodic messages to the **Message Manager** window to indicate its status. The **Message Manager** window also lists any errors or warnings encountered during the analysis.

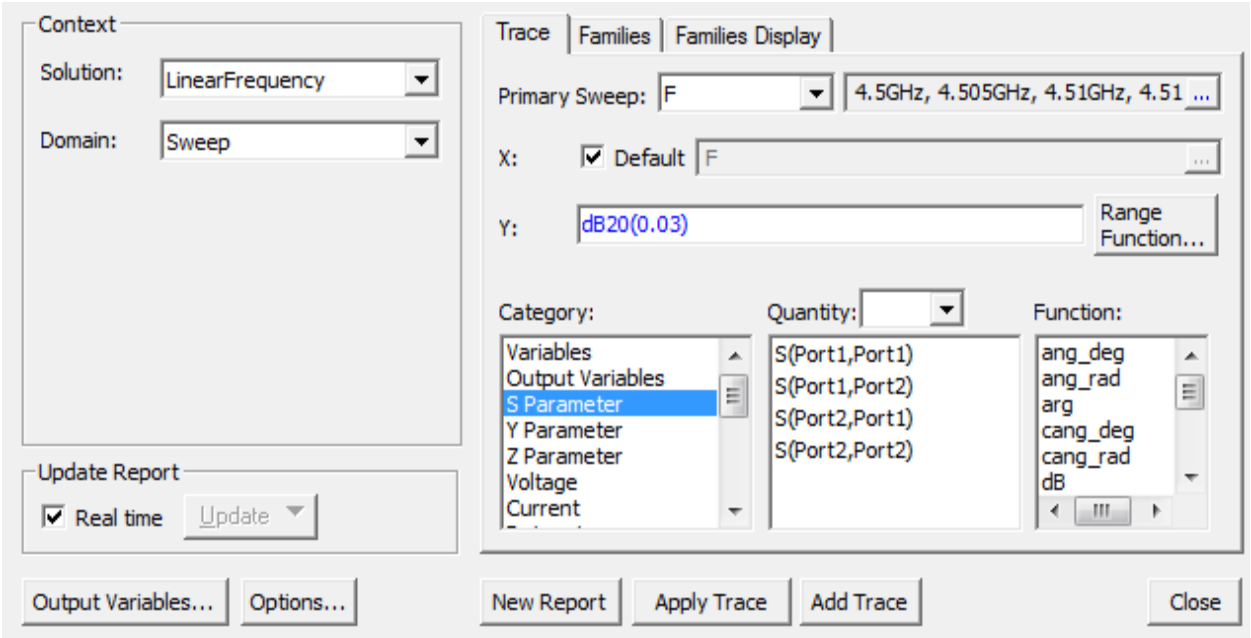
The next step is to generate an analysis report.

Generate an Analysis Report

To view your simulation data, create a report. A wide variety of report types can be created in **Electronics Desktop**. To create a report, right-click **Results** in the **Project Manager** window and select the type of report you want to create.



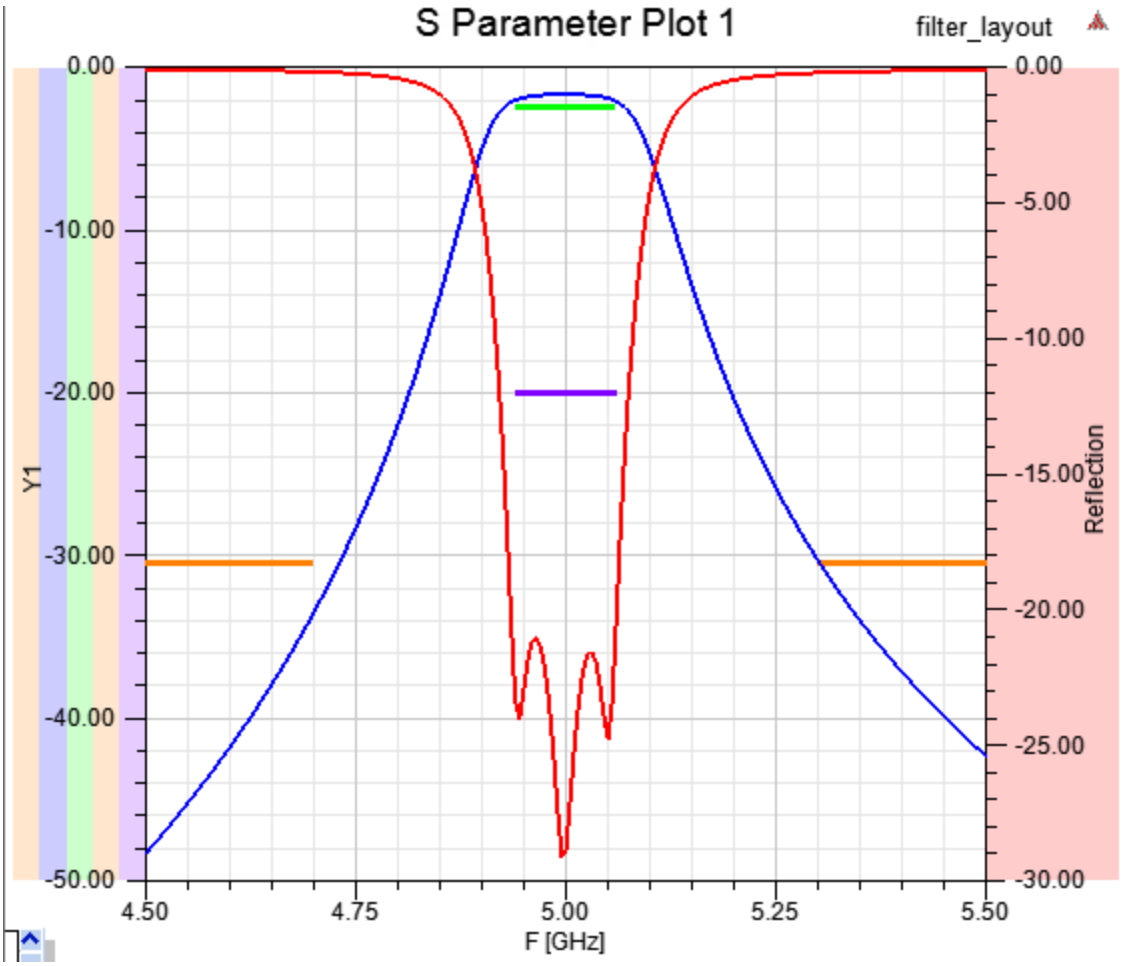
A **Report** creation window appears letting choose parameters to plot and functions to apply.



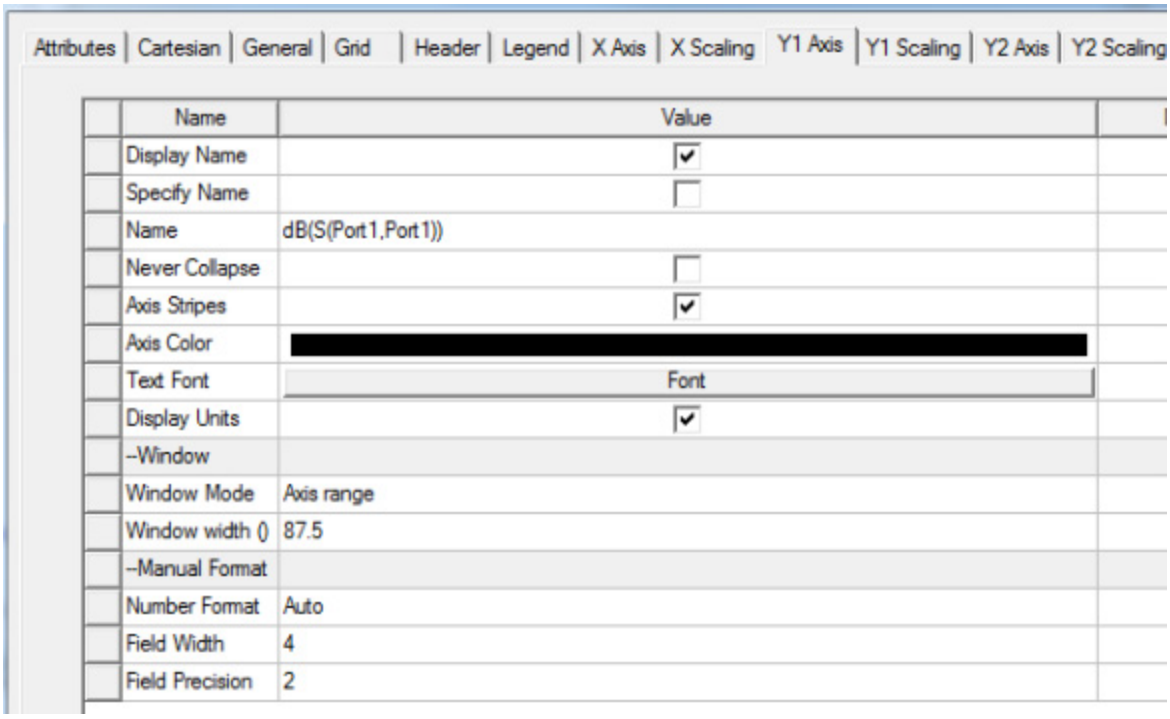
- You can select more than one quantity at a time if you wish to plot several results on the same graph.
- Click the **ApplyTrace** or **AddTrace** buttons to change your plot, if appropriate.

- Click **NewReport** to create the report.
- Close the **Report** creation window if you are happy with the result.

A wide range of customization options are available for the generated plot.



Click on different parts of the report, or click on traces in the **Project Manager** window, to change properties in the **Properties** window. For example, clicking the Y axis in the report window gives the following options. Clicking different parts of the plot yields different options.



This concludes the demonstration of the overall framework for using **Electronics Desktop** for circuit and system analysis.

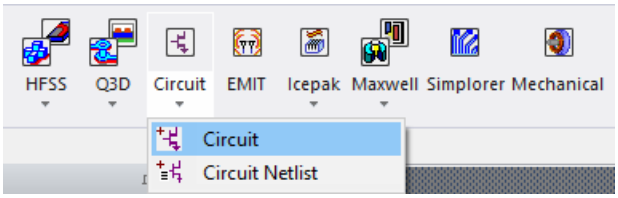
3 - Basic Transmission Line

This chapter contains the following topics:

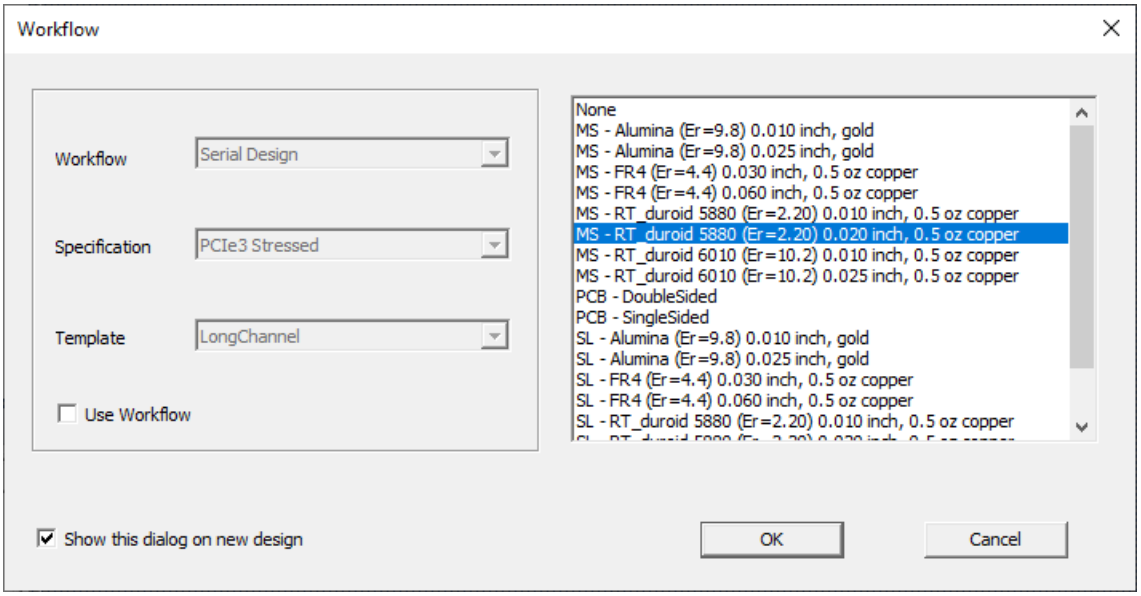
Launch Ansys Electronics Desktop

Complete the following steps to create a circuit schematic of a basic transmission line, define a setup, run an analysis and perform post-processing, using **Electronics Desktop**.

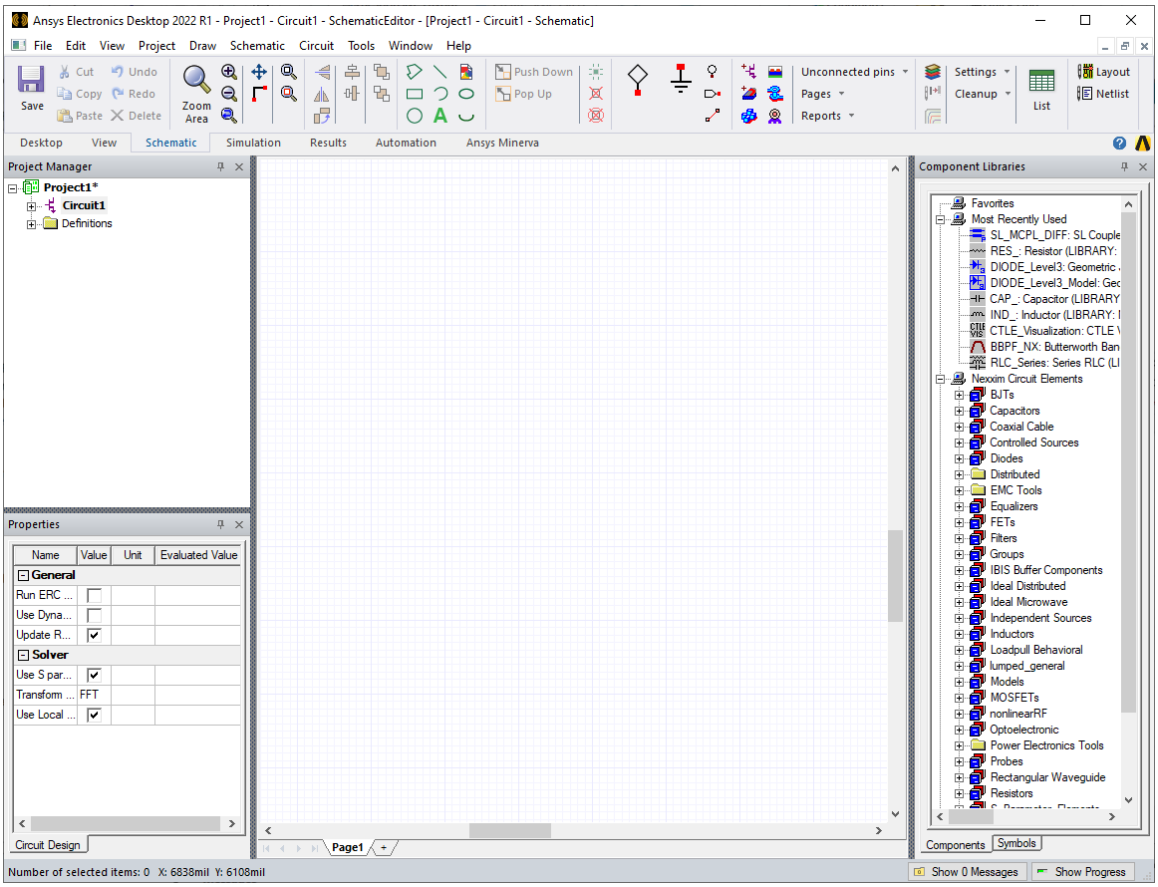
1. Open **Electronics Desktop**.
2. From the **File** menu, select **New** to start a new project.
3. From the **Project** menu, select **Insert Circuit Design**, or select **Circuit** > **Circuit** on the **Design** ribbon to open the **Workflow** window.



4. Select **MS – RT Duroid 5880 (Er=2.20) 0.020 inch, 0.5 oz copper** and click **OK**.



5. Click **OK** to open the new Circuit Design project.



The next step is to explore the **Project Manager** window.

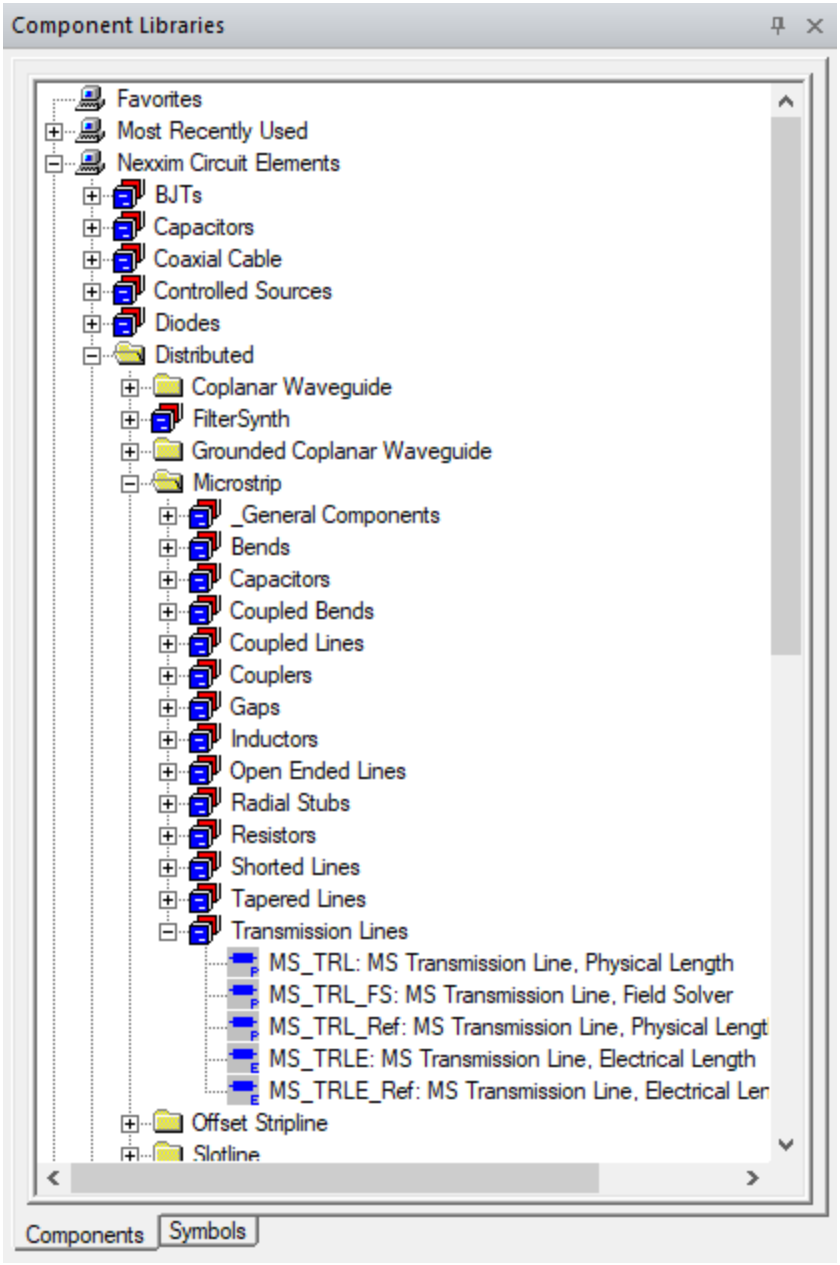
Project Manager Window

The **Project Manager** window lists all the designs that make up a project. expand the **Project Tree** and the **Circuit***n* design folder. The **Data** folder contains information about the Substrate data. The **Analysis** folder contains information about analysis setups, such as freq sweeps, power sweeps, and variable sweeps. The **Project Manager** window can be used to view and edit information in these folders.

Add a Transmission Line

1. Click **View** > **Components Libraries** to open the **Component Libraries**.
2. Click the **Components** tab.

3. Expand **Nexxim Circuit Elements** > **Distributed** > **Microstrip** > **Transmission Lines**.



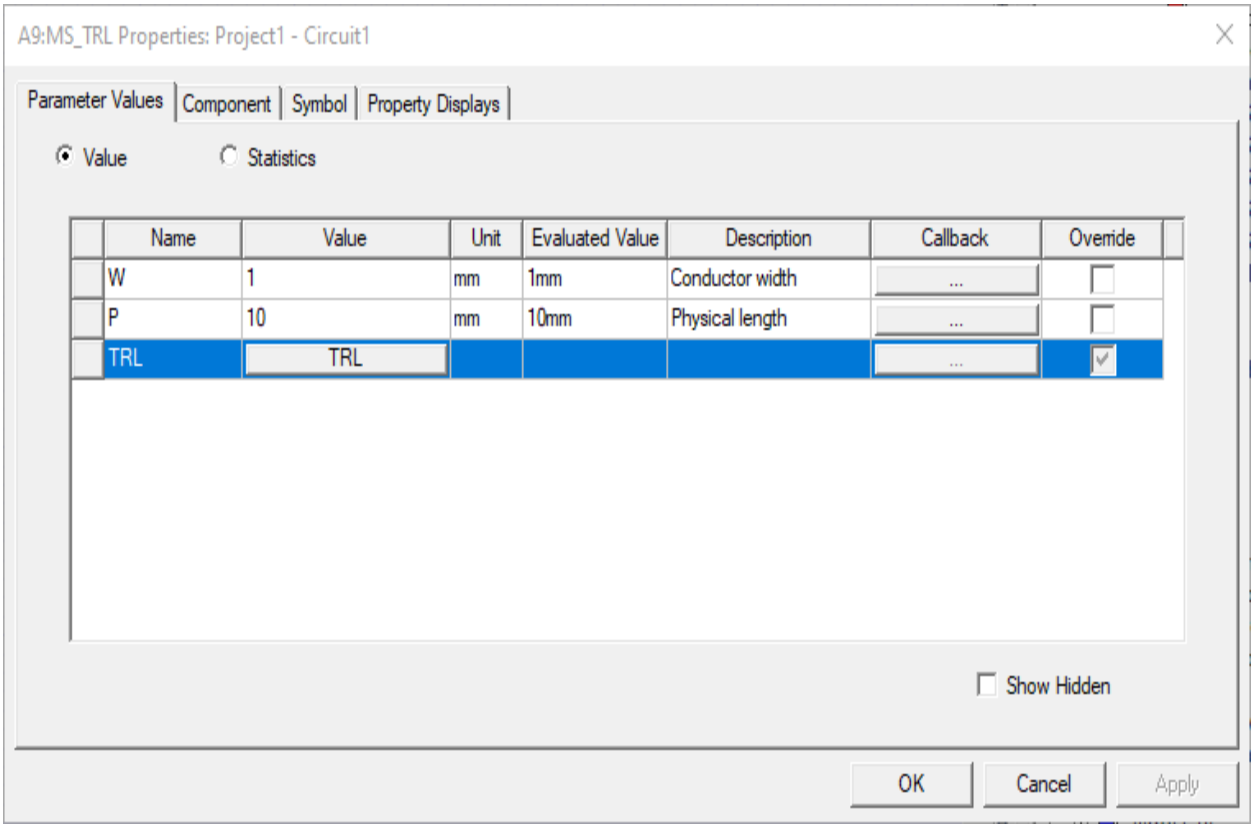
4. Double-click the **MS_TRL:MS Transmission Line, Physical Length** component.
5. Move the cursor over to the schematic.
6. Click anywhere to place the transmission line in the schematic and press **Esc**.

The next step is to synthesize a 50 ohm TRL.

Synthesize a 50ohm TRL

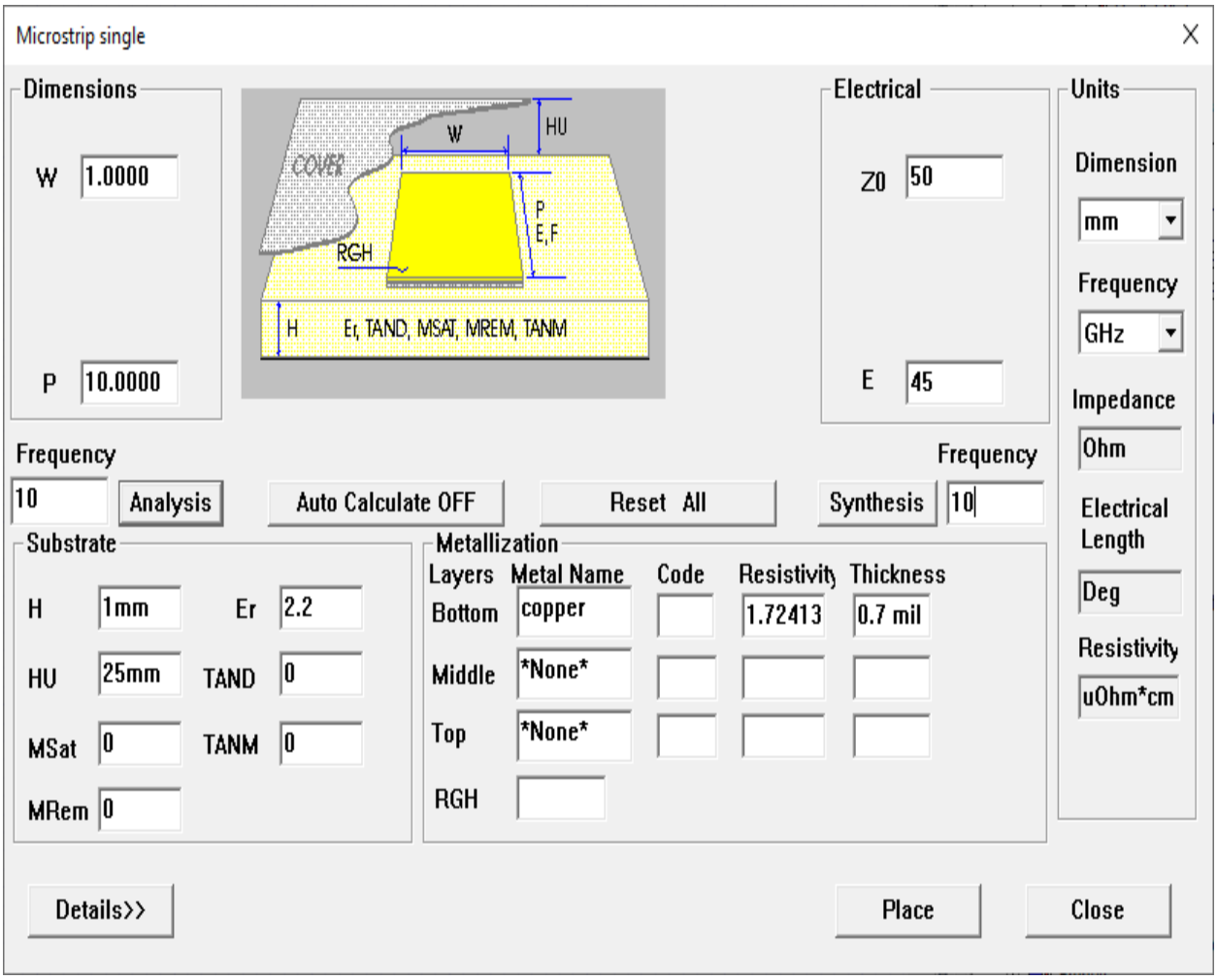
> **Note:** While performing these steps, you may encounter a **Merge Layer** window. For more information, refer to the Merge Layers section following step 6.

1. Double-click the **Transmission Line** in the Schematic window to open the component's **Properties** window.



2. In the **TRL** row, click the **TRL** Value field to open the **Microstrip single** window.

> **Note:** Depending upon You may or may not see a **Merge Layer** window appear. For more information, see the Merge Layers section in the follow figure.



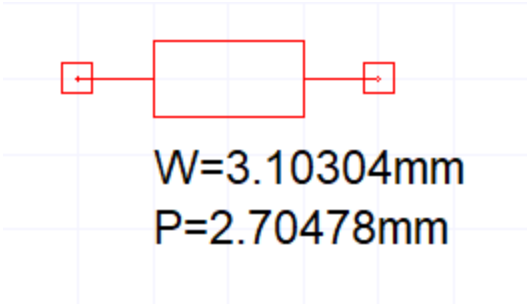
3. In the **Frequency** field to the right, enter **10**.

> **Note:** By default, **Z0** = 50.

4. Click **Synthesis**.

> **Note:** The **Dimensions** are automatically filled in for **W** (width) and **P** (physical length) for a 50 ohm TRL.

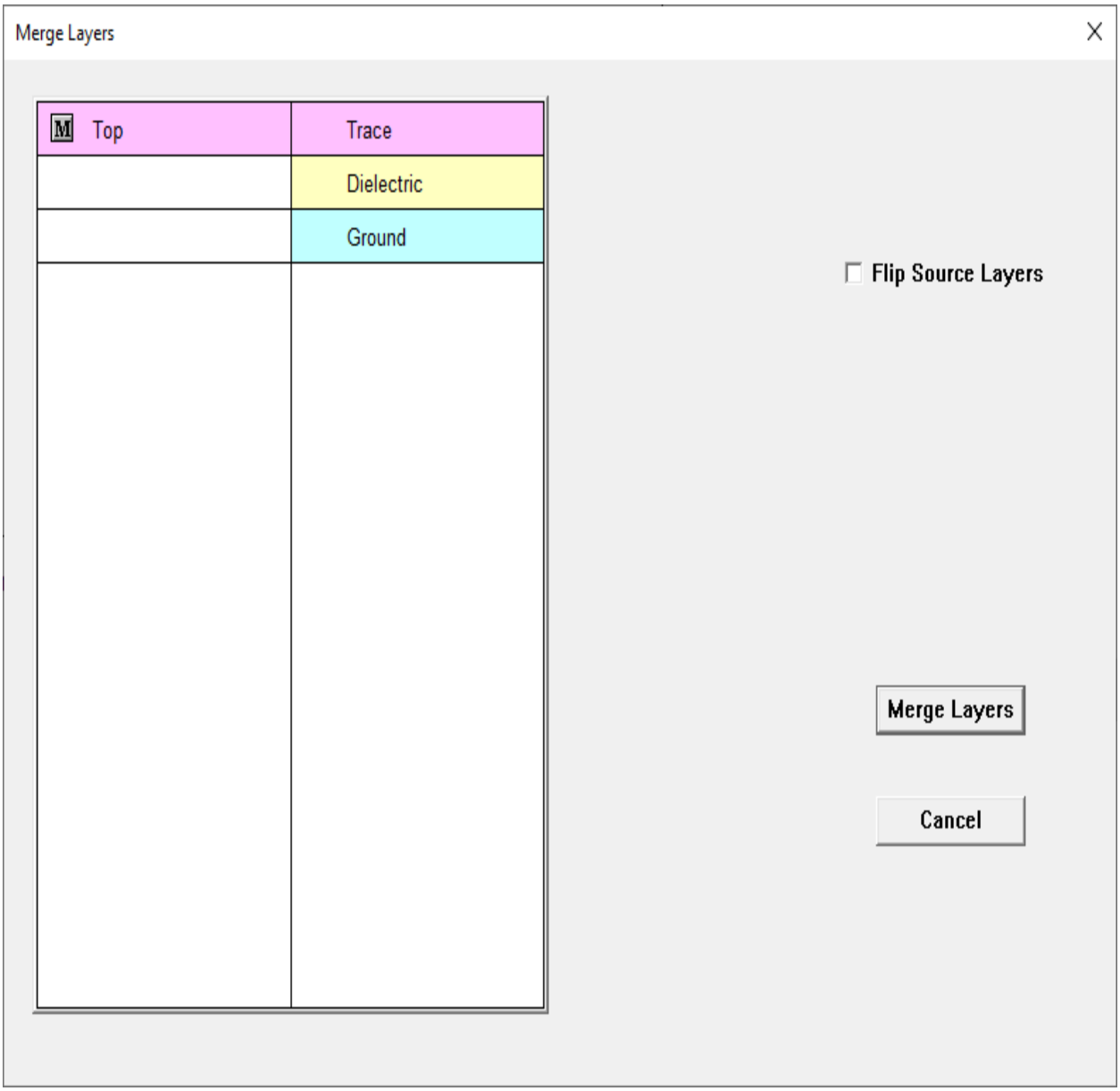
5. Click **Place**.
6. From the **Properties** window, click **OK**.



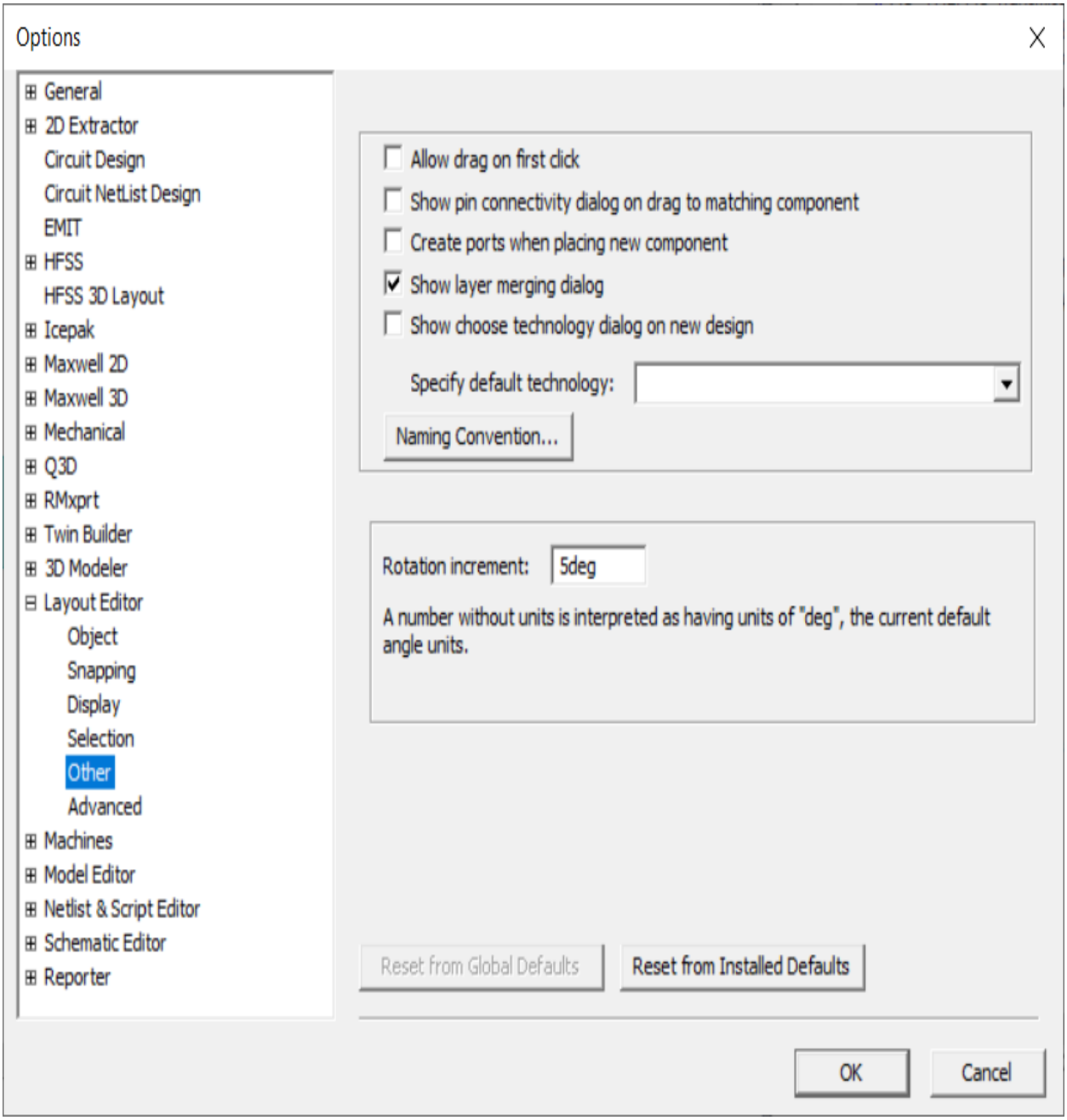
The transmission line dimensions are automatically placed into the schematic component.

Merge Layers Window

Depending upon the configuration of the design and whether **Show layer merge dialog** is enabled in the global **Options** window, you may see the **Merge Layers** window. **Show layer merge dialog** is unchecked (deactivated) by default.



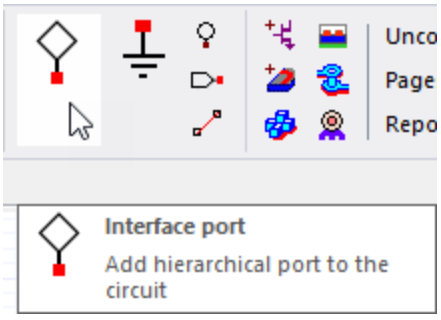
To enable the **Merge Layers** window, navigate to **Tools** > **Options** > **General Options ...**. Then expand the **Layout Editor** menu and select Other. Finally, fill the check box next to **Show layer merge dialog** to enable the window.



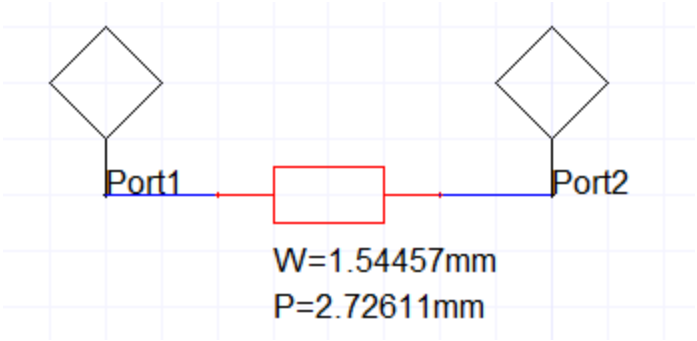
The next step is to add ports.

Add Ports

1. From the toolbar, click the **Interface Port**.



2. To place the ports, click the left and right terminals of the transmission line to place the ports.

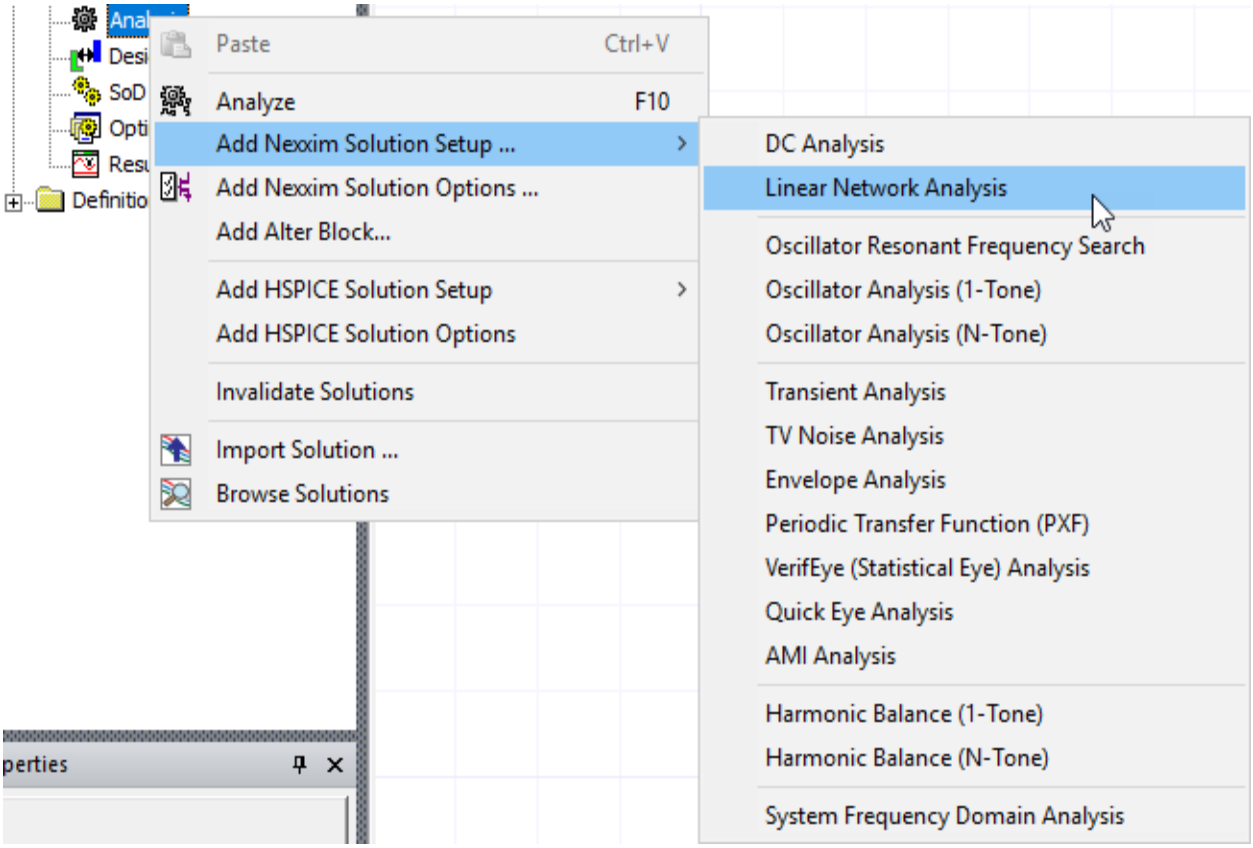


3. Press Spacebar to finish placing the components.

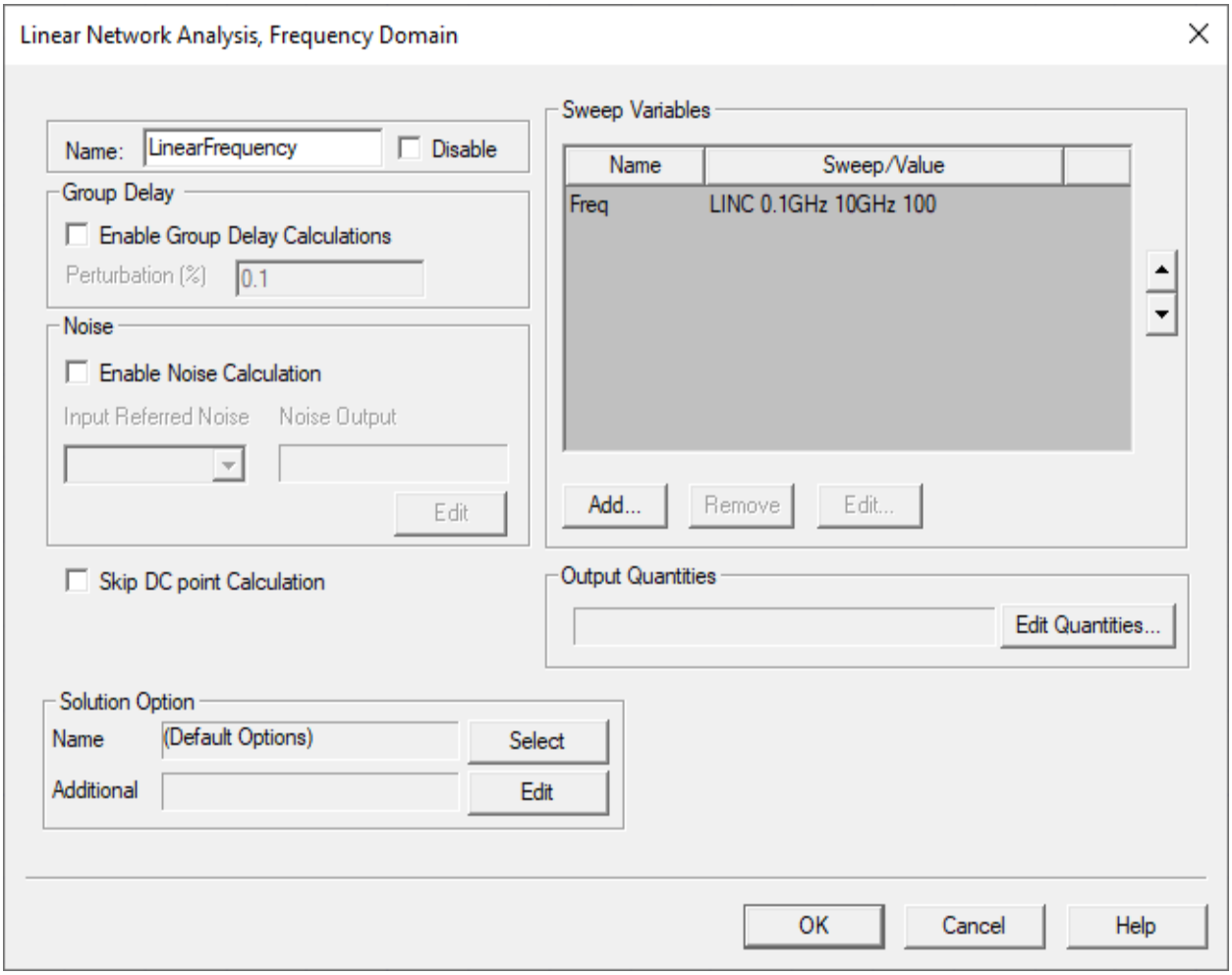
The next step is to add and run an analysis.

Add and Run an Analysis

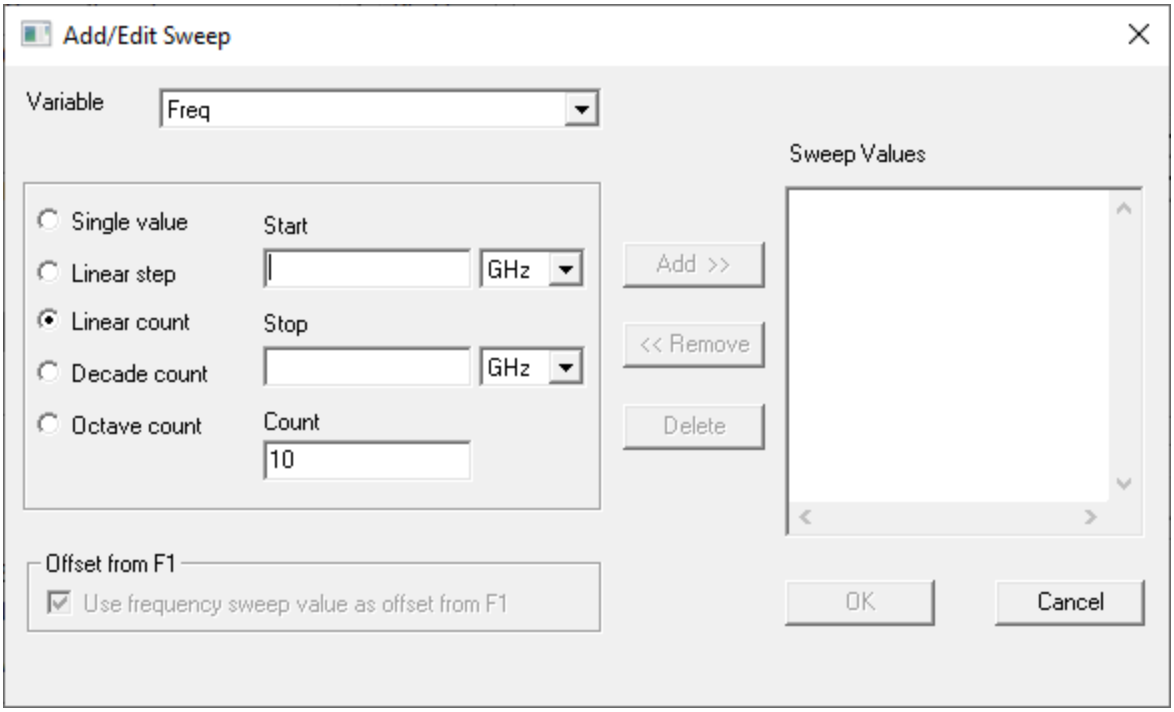
1. From the **Project Manager** window, right-click **Analysis** and select **Add Nexxim Solution Setup ... > Linear Network Analysis**.



2. In the **Linear Network Analysis** window, click **Add**.



3. In the **Add/Edit Sweep** window:
   a. Select **Linear Count**.
   b. Set **Start** to **0**, **Stop** to **10 GHz**, and **Count** to **400**.
   c. Click **Add>>** and **OK**.



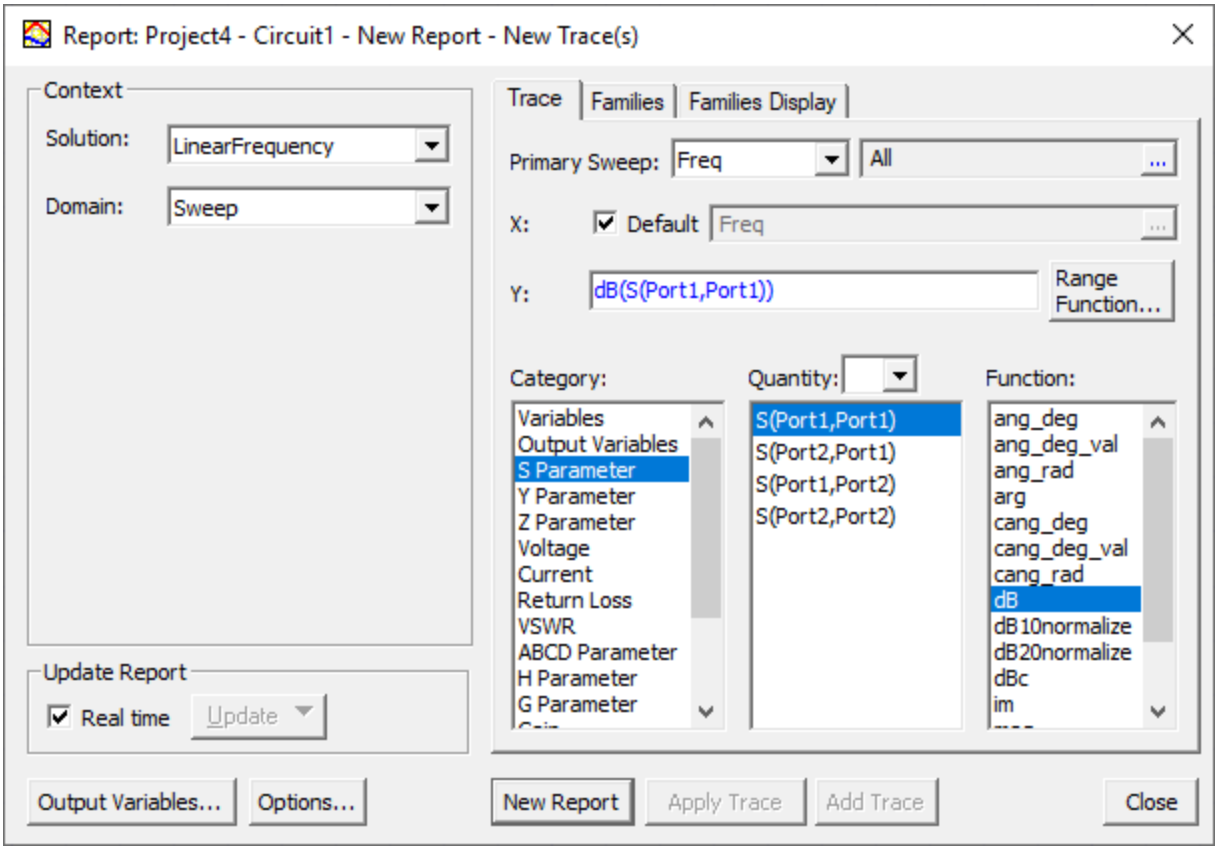
4. In the **Linear Network Analysis/Frequency Domain** window, click **OK**.
5. Save the project.
6. From the **Project Manager** window, expand **Analysis**.
7. Right-click the analysis setup **LinearFrequency** and select **Analyze**.

The next step is to plot the results.

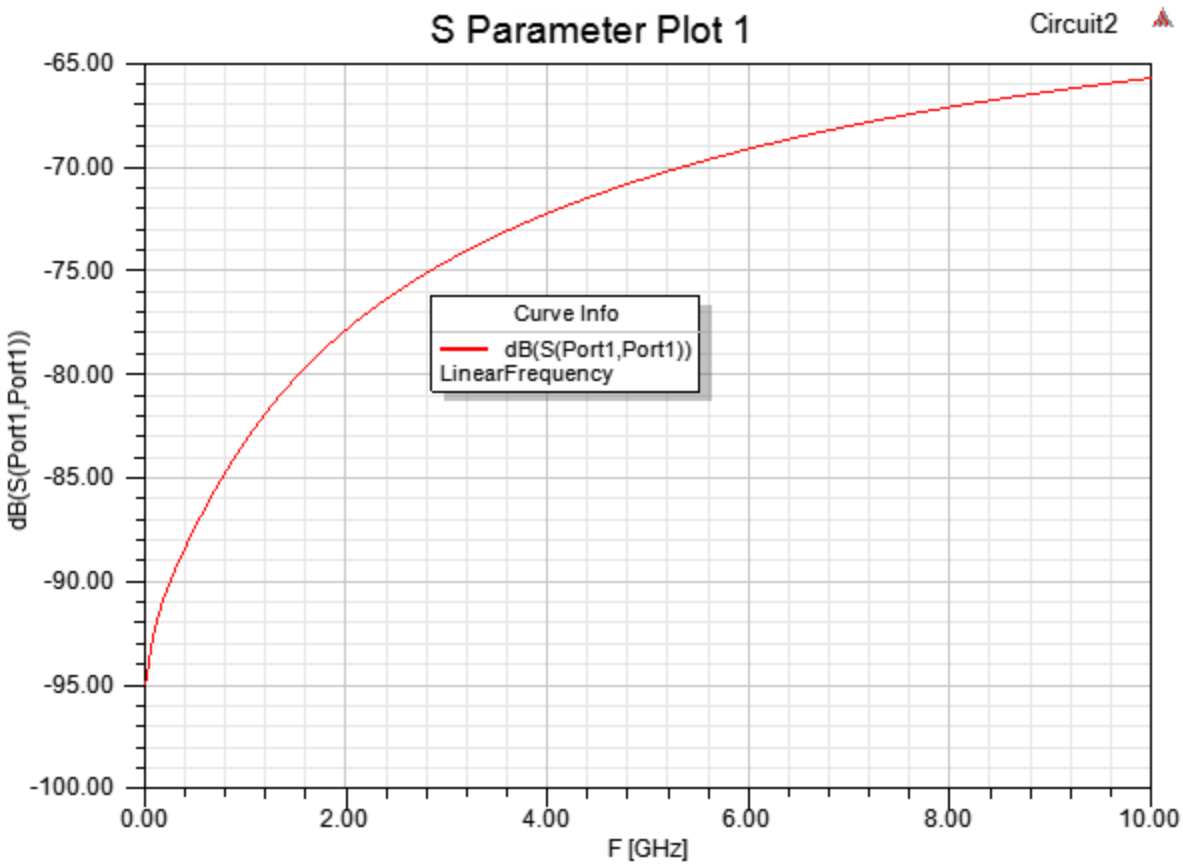
Plot Results

1. From the **Project Manager** window, expand the **Project Tree** and [*active design folder*]. Then right-click the **Results** folder and select **Create Standard Report** > **Rectangular Plot** to open the **Report** window.
2. In the **Report** window, set:

- **Category** to **S-Parameters**
- **Quantity** to **S(Port1, Port1)**
- **Function** to **dB**



3. Click **New Report** and **Close**.
   The report is created.

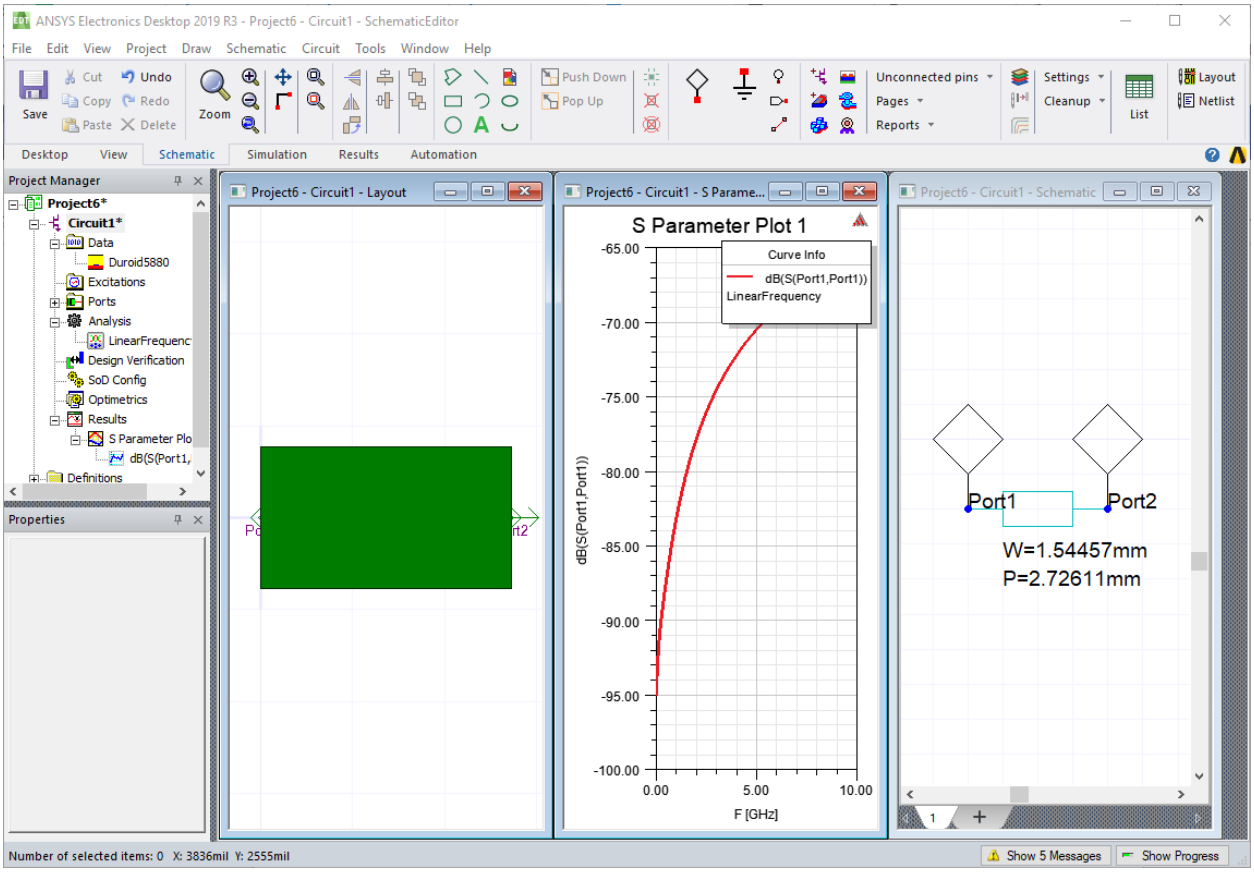


The next step is to open the Layout Editor.

Open Layout Editor

1. From the **Project Manager** window, right-click the design name (**Circuit***n*) and select **Layout Editor** to open the **Layout** window.
2. Click **Window** > **Tile Vertically**.

This step vertically arranges the open windows: layout, plot, and schematic of the transmission line.



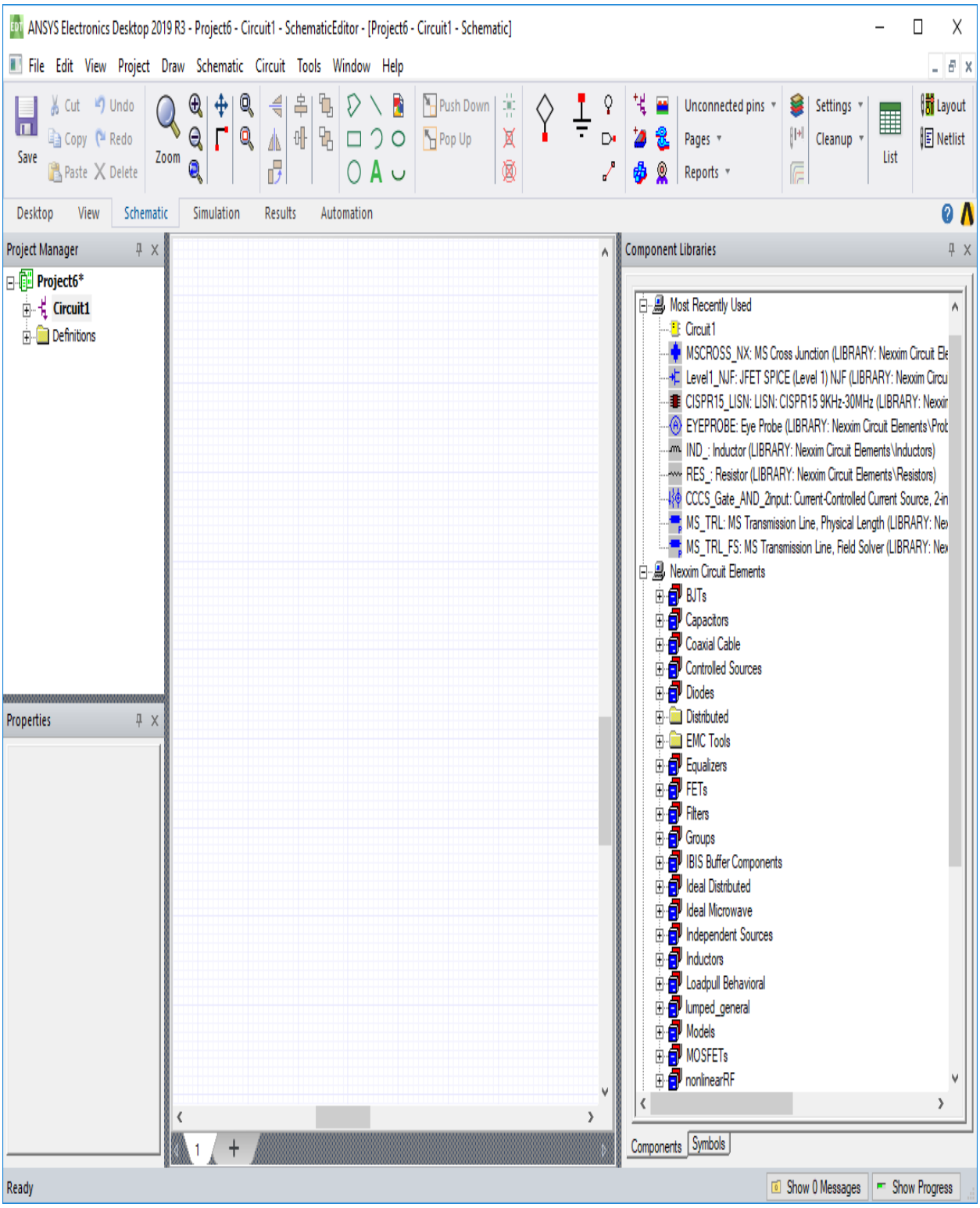
You now know how to design a basic transmission line, analyze it, and view its information in multiple windows simultaneously.

4 - Simple Mixer

This chapter contains the following topics:

Circuit Design in Electronics Desktop

In the Ansys Electronics Desktop, you can simulate high-speed, high-density circuit designs. Analyses can be provided in the time and frequency domains for all levels of projects, from individual transistor models to large-scale integrated devices and communication channels.



This section and the next introduce Circuit Designs by showing how to create and run the following analyses:

- A mixer with Transient and Harmonic Balance (HB) analyses.
- A communication channel with VerifEyeAnalysis and Quick Eye Analysis setups.

Learn:

- how to create the two circuit designs with the schematic editor.
- how to set up and run Transient, Harmonic Balance, QuickEye, and VerifEye analyses.
- how to display simulation results using Circuit Design reporting functions.

Both circuits are available in the Examples directory.

Simple Mixer Example

For this example, run transient and harmonic balance analyses of a mixer circuit, a common task in RF design. As you work through this topic, learn how to:

- Open the example circuit on the Examples directory.
- Alternatively, create the simple mixer circuit using the **Schematic Editor**.
- Set up and run transient and harmonic balance analyses.
- Create reports for the time and spectral results.

After setting up the schematic, run the simulations and perform post-processing.

The topics for this example are:

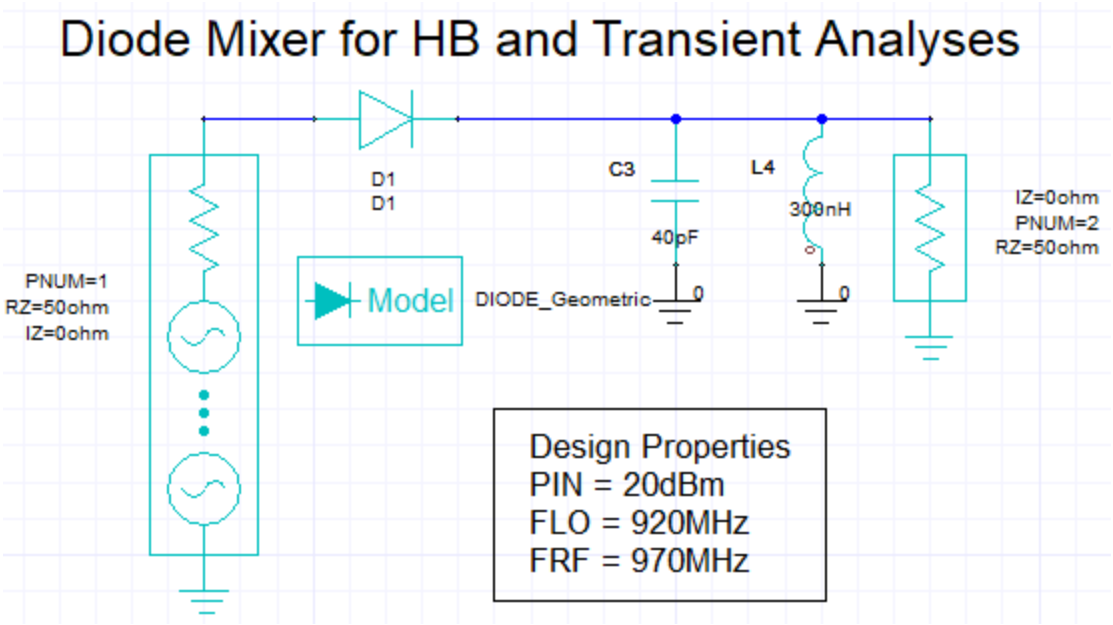
Open Simple Mixer Project on the Examples Directory

After you launch Ansys Electronics Desktop, open the simple mixer project on the Examples directory as follows:

1. From the **File** menu, select **Open Examples**. The explorer window appears, in the **Examples** directory.

2. Expand the **Circuit** directory, then the **RF Microwave** > **Mixers** directories, and finally select the file **SimpleMixer.aedt**. Click **Open**.

The **Schematic Editor** window opens to display the mixer schematic.

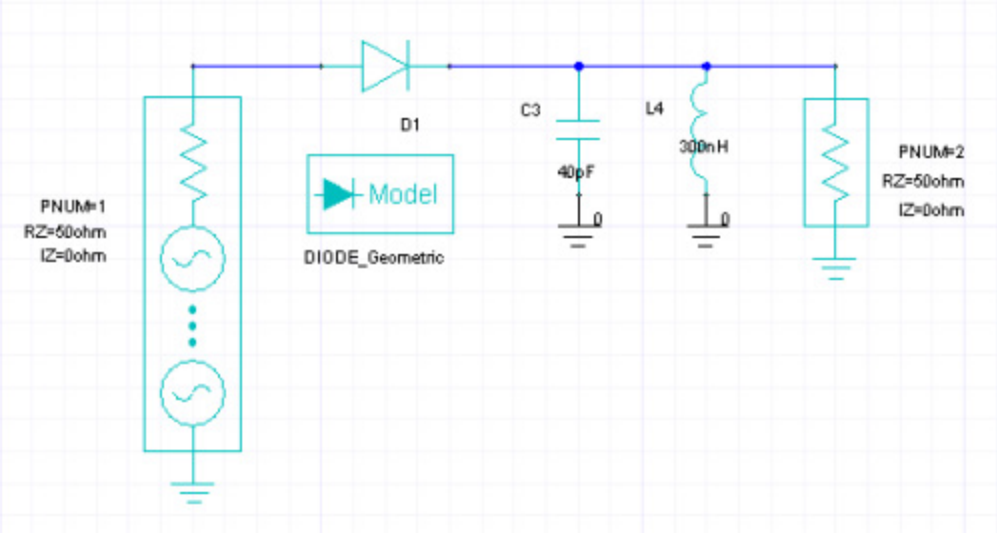


A mixer typically multiplies sinusoidal signals of different frequencies to achieve frequency translation. In this example, input port Port 1 includes two power sinusoidal sources. The lower frequency FLO (for Local Oscillator) acts as a carrier, modulated by the higher frequency FRF. The output at Port 2 can be viewed in the time domain.

Note: The following topics show how to create this Simple Mixer circuit with the **Schematic Editor**.

Create Simple Mixer with Schematic Editor

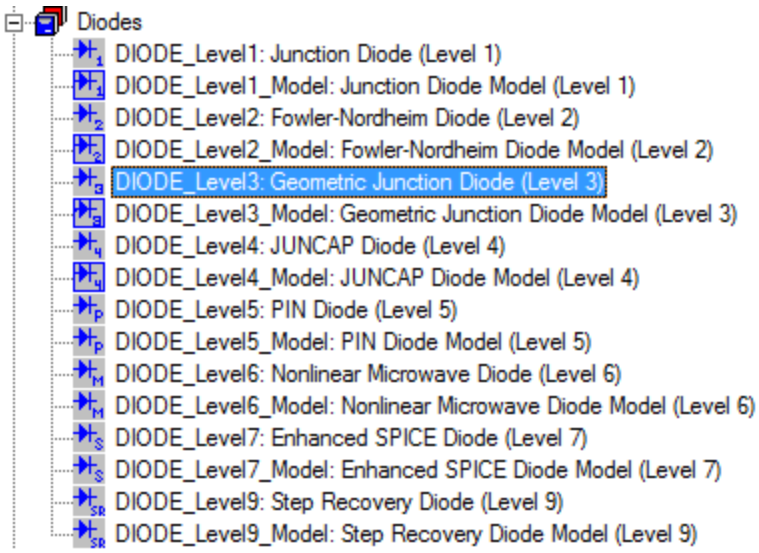
Instead of opening the example file, use ANSYS Electronics Desktop's **Schematic Editor** to create the mixer schematic for simulation. The following circuit is created.



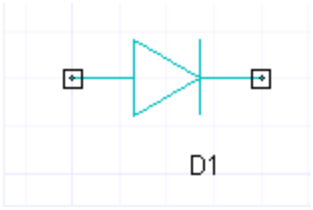
A mixer typically multiplies sinusoidal signals of different frequencies, achieving frequency translation. In this example, input port Port 1 includes two power sinusoidal sources. The lower frequency FLO (for Local Oscillator) acts as a carrier, modulated by the higher frequency FRF. The voltage at Port 2 can be viewed in the time domain.

To create the design, follow these steps:

1. Launch **Electronics Desktop**. A new project, **Project*n***, should appear (***n*** is the order in which the project was added to the current session of Ansys Electronics Desktop).
2. If no project appears, create one. Click the **File** drop-down menu and select **New**. A new project named **Project*n*** is added to the **Project Tree**.
3. From the **Project Manager** window, expand the **Project Tree**. Then right-click the project and select **Rename**. Our example has been renamed to **SimpleMixer**.
4. From the **Project** menu at the top of the **Electronics Desktop** window, select **Insert Circuit Design** to open the **Workflow** window.
5. Click **None** to open the **Schematic Editor** window with an empty design window.
7. Go to the **Component Libraries** window. Scroll down to and expand the **Diodes** folder by clicking on the plus sign symbol. If you do not see the Component Libraries window, go to **View** and select the **Component Libraries** option.

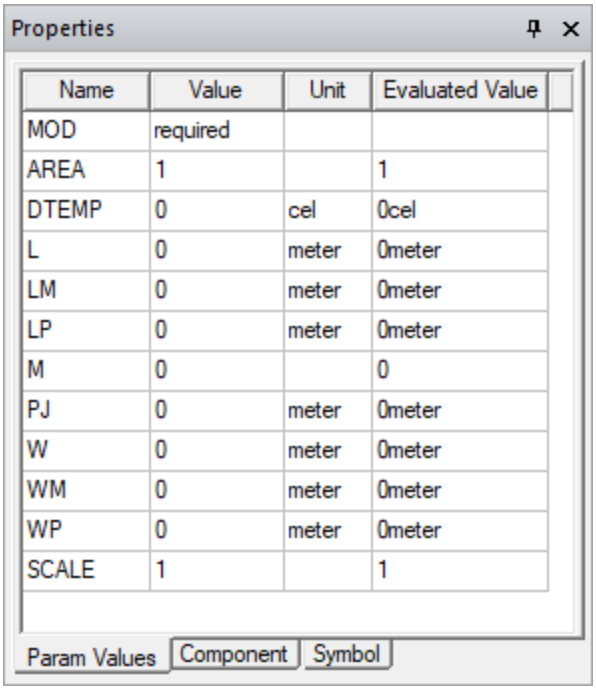


8. This circuit uses the Level 3 Geometric Junction Diode model. **Click+drag** the **DIODE_Level3:** element into the design window.
9. Release the mouse button to drop the symbol and press **Esc** to avoid dropping a second diode.



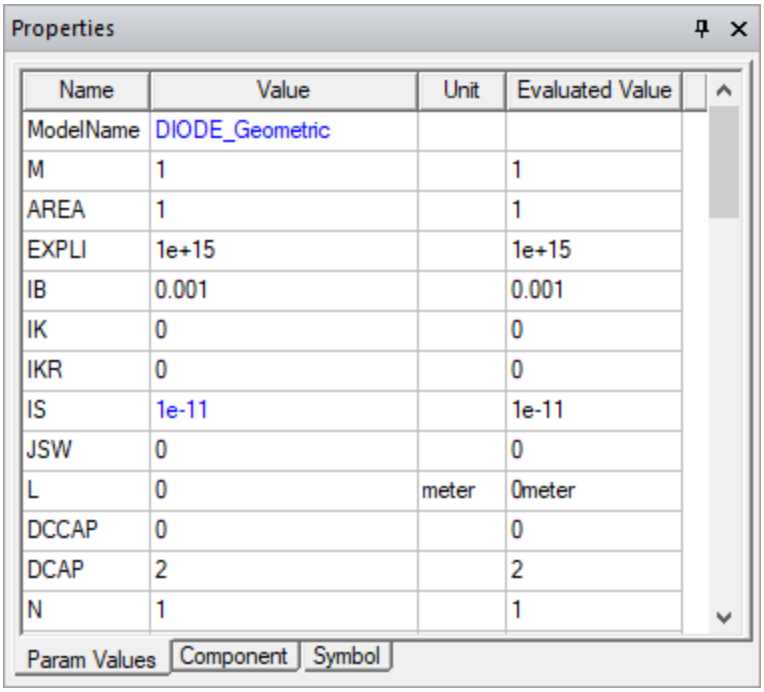
The reference designator **D***n* is automatically assigned. The *n* is incremented each time a component is added to the design.

9. Click the diode symbol to display its properties in the **Properties** window **Param Values** tab.



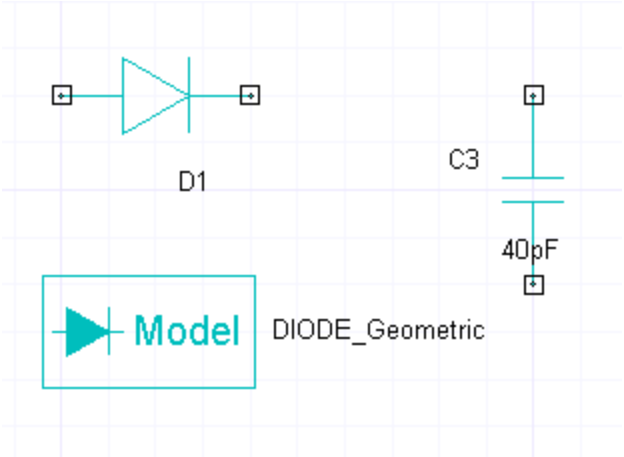
10. Set the **MOD** Value field to the name of the diode model you intend to use. In the following screenshot, **DIODE_Geometric** is used as the name. Use the same name for the diode model to connect the instance and the model.
11. In the **Components Libraries**, **click+drag** the **DIODE_Level3_Model:** element into the design window. A diode model symbol is dragged into the window. Locate the model symbol beneath the diode symbol. Release the mouse button to drop the model symbol and press **Esc**.
12. Click the diode model symbol to display its properties in the Properties tab. Set the **ModelName** Value field to **DIODE_Geometric**. Set the **IS** Value field (saturation current)

to **1e-11** (amperes).



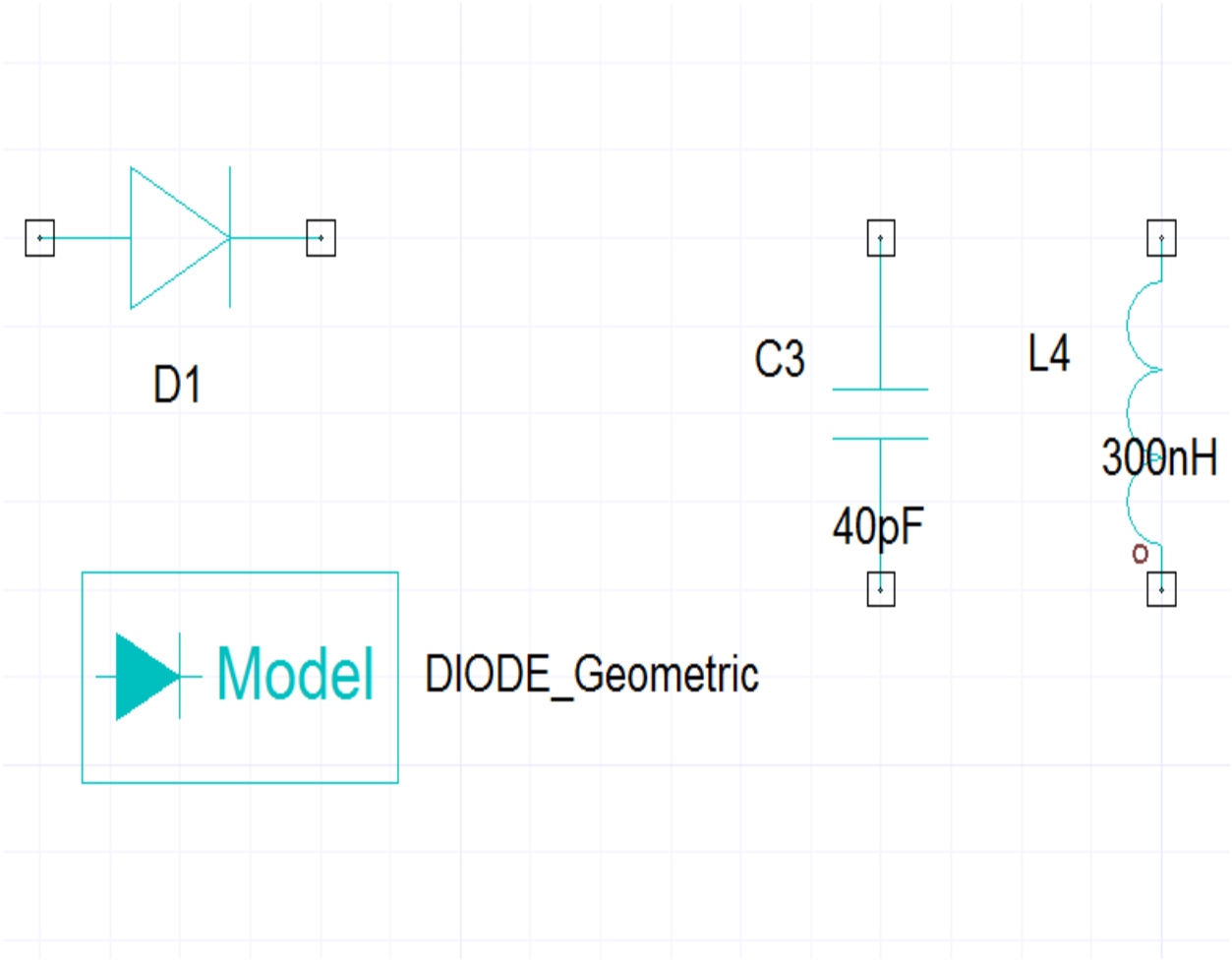
13. In the **Components Libraries**, expand the **Capacitors** folder. Click the **CAP_:** element and drag the capacitor symbol into the design window. Locate the capacitor to the right of the diode. Press **Enter** to drop the capacitor symbol.
14. Select the capacitor symbol to display its properties. Set the **C** Value field to **40pF**.
15. With the capacitor symbol still selected, press **Ctrl** +**R** to rotate the symbol into a vertical position. Move the capacitor symbol so its upper terminal is aligned with the output of the diode.

The schematic should look like:



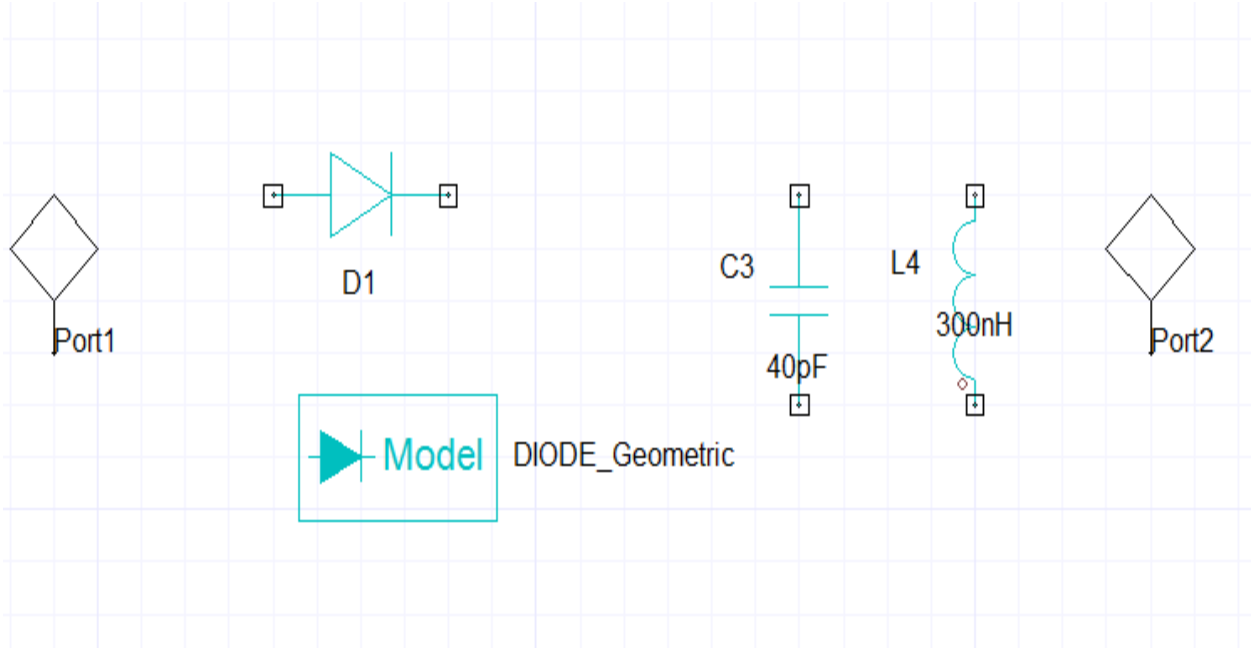
16. In the **Components Libraries**, expand the **Inductors** folder. Click the **IND_:** element and drag the inductor symbol into the design window. Press **Enter** to drop the inductor symbol.
17. Select the inductor symbol to display its properties. Set the **L** Value field to **300nH**.
18. With the inductor symbol still selected, press **Ctrl** +**R** to rotate the symbol into a vertical position. Position the inductor symbol to the right of the capacitor. The schematic so far

should look like:

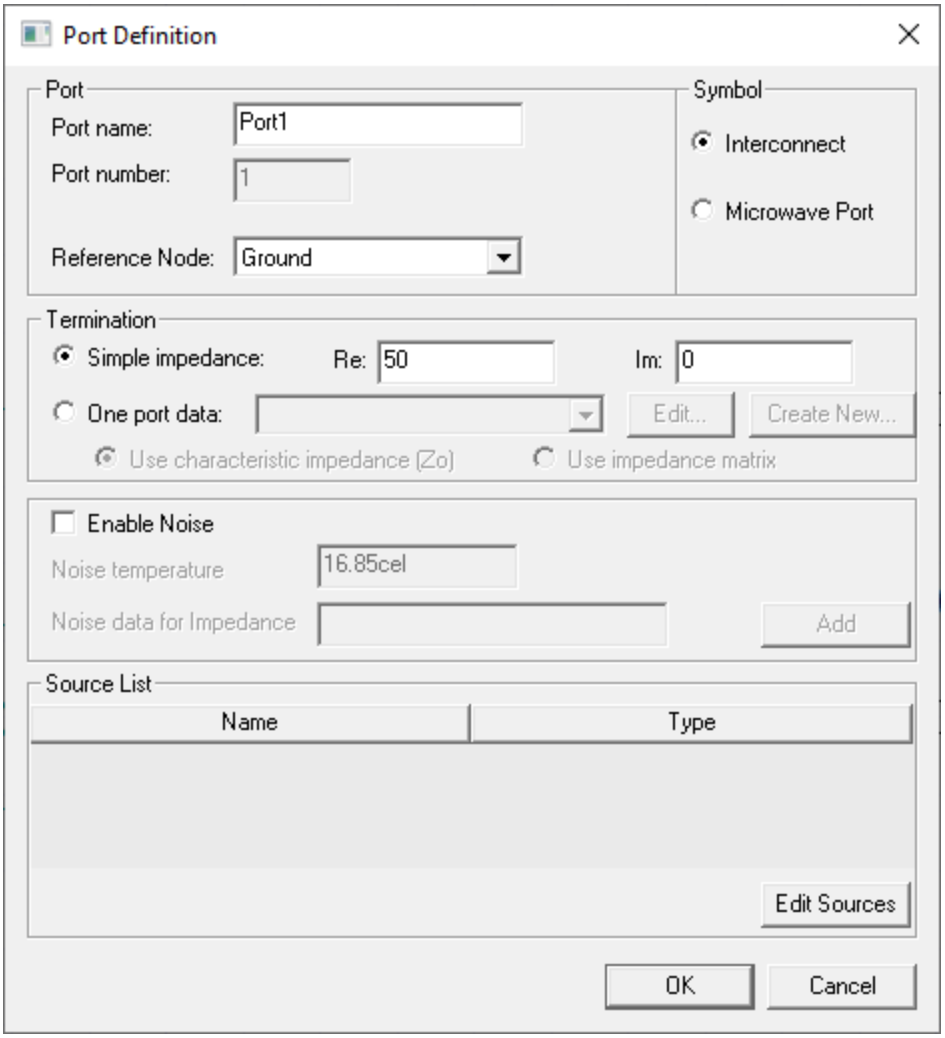


19. Click the interface port icon  in the upper-right ribbon area.

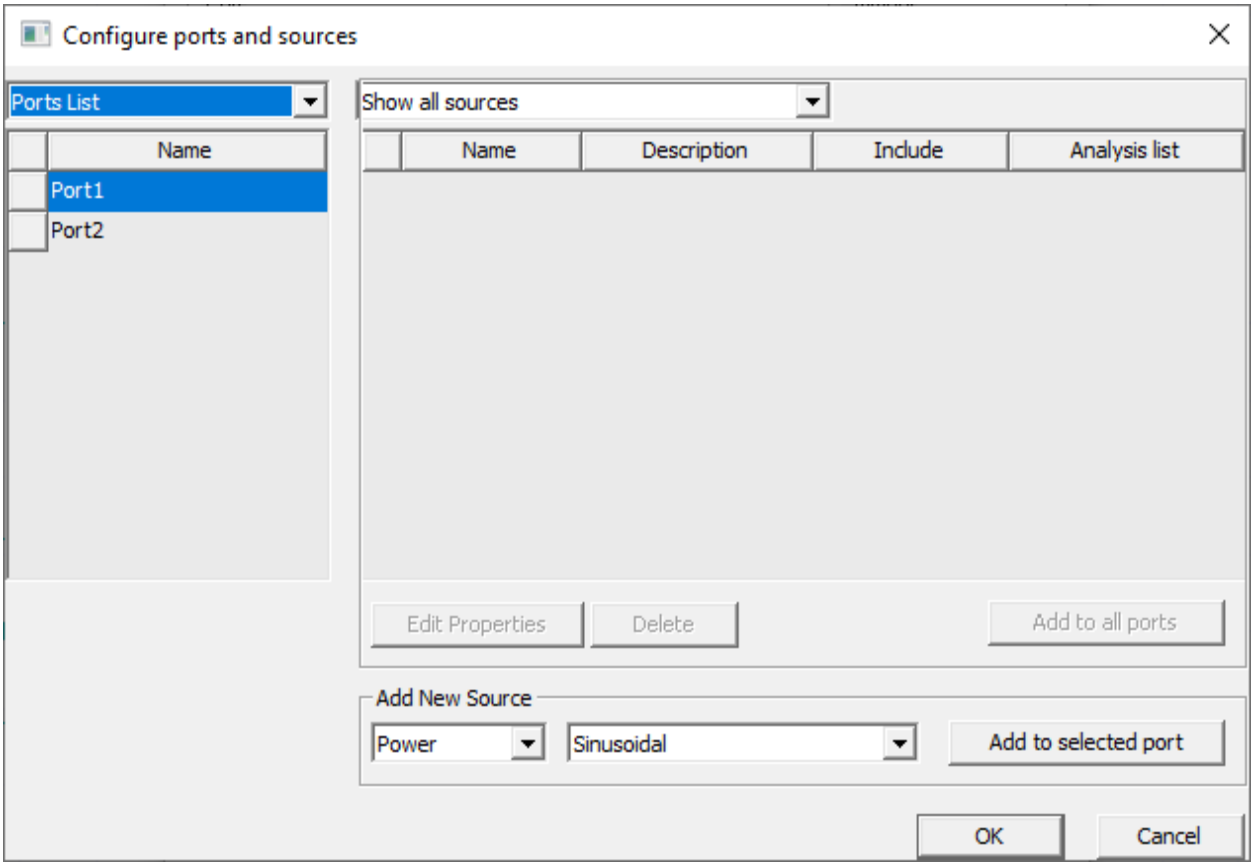
Place one port to the left of the existing elements, and a second port to the right. In our example, the input port is Port 1 and the output port is Port 2.



20. Right-click the input port and select **Edit Port**. The **Port Definition** window appears:

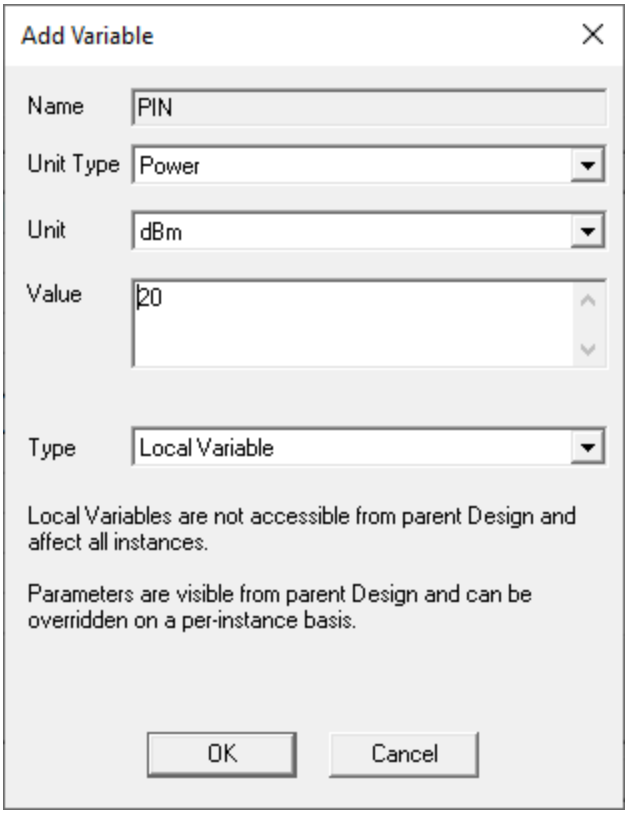


21. Select the **Microwave port** symbol.
22. Accept the default termination of 50 ohms.
23. Click **Edit Sources** to open the **Configure ports and sources** window.



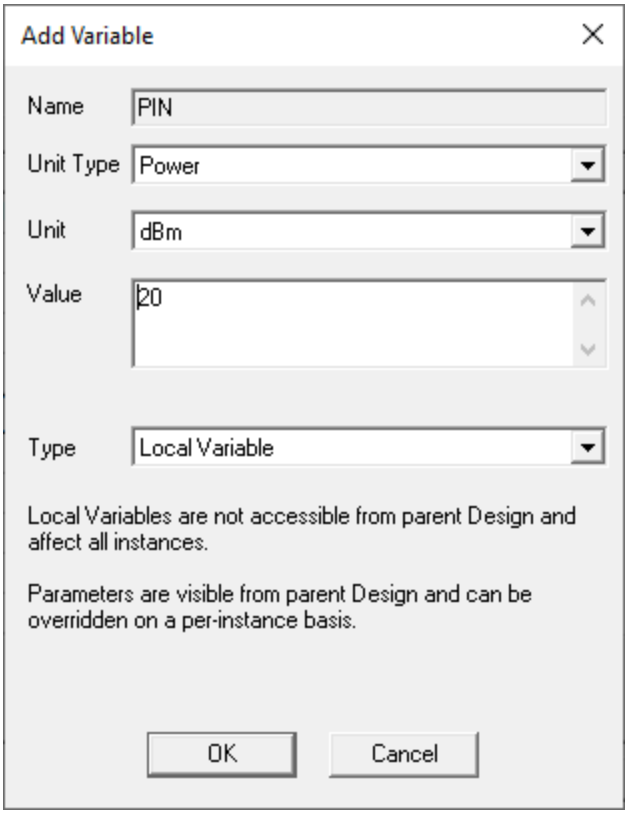
24. **Port 1** is selected in the **Ports List**. **Power** and **Sinusoidal** are the default source parameters. To add a new power sinusoidal source to the port, click **Add to selected port** to open the **Properties** window. The three properties of interest are the **POWER**, **FREQ**, and **TONE** parameters. Use local variables for the power and frequencies of the sources, making it easier to modify these parameter values between simulations.
25. Set the **POWER** drop-down menu to **PIN** and press **Enter**. The **Add Variable** window

appears:



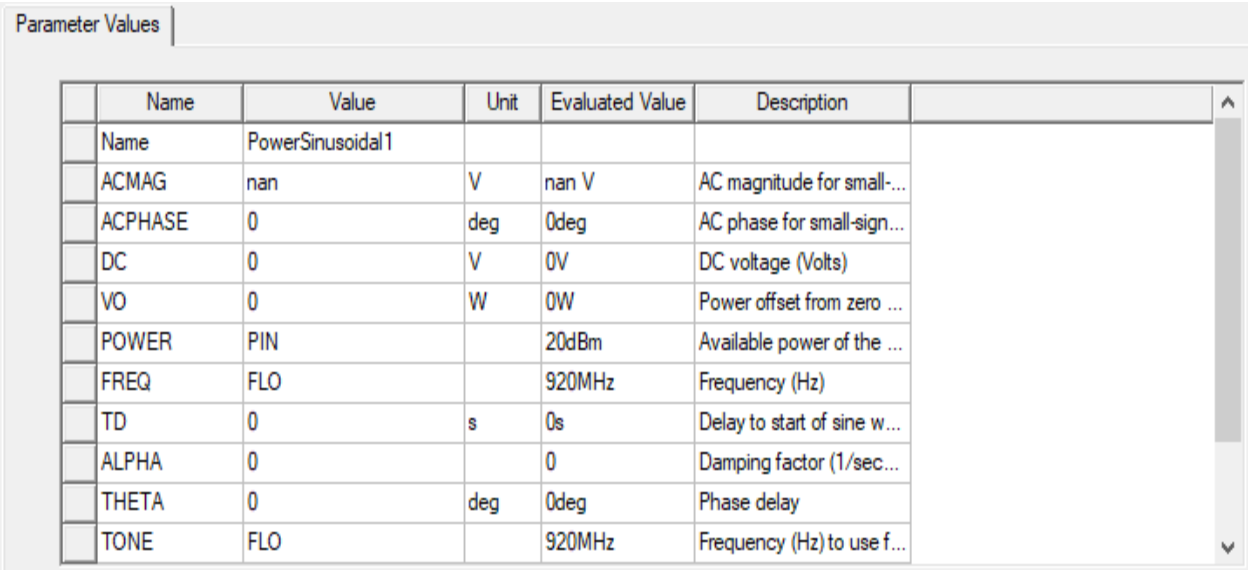
Set the **Unit Type** to **Power**, the **Unit** to **dBm**, and the **Value** to **20** as shown. Click **OK**.

26. Set the **FREQ** Value field to **FLO**. The **Add Variable** window opens:



27. Set the **Unit Type** to **Frequency**, the **Unit** to **Hz**, and the **Value** to **920MHz** as shown. Click **OK**.
28. Set the **TONE** Value field to **FLO**. This value is used by harmonic balance.

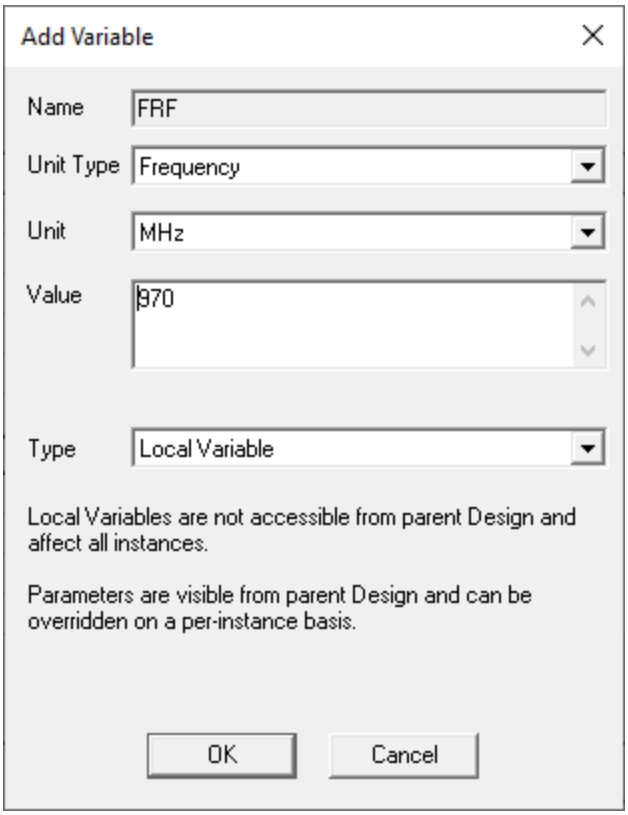
The **Parameter Values** tab on the **Properties** window for the Power Sinusoidal1 source should look like:


Parameter Values

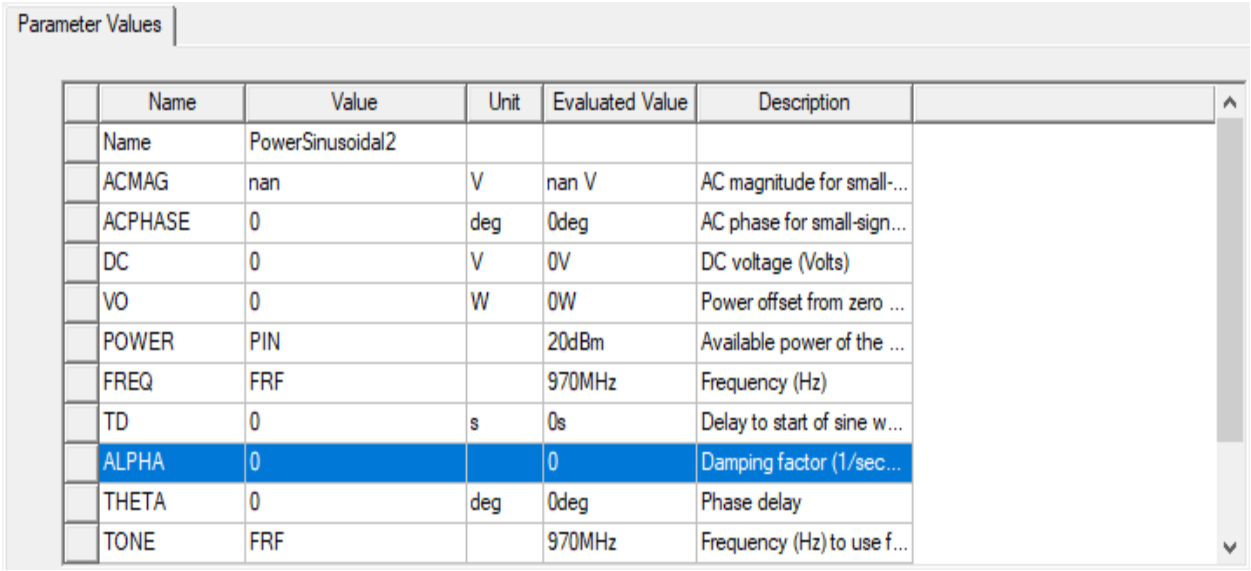
	Name	Value	Unit	Evaluated Value	Description
	Name	PowerSinusoidal1			
	ACMAG	nan	V	nan V	AC magnitude for small-...
	ACPHASE	0	deg	0deg	AC phase for small-sign...
	DC	0	V	0V	DC voltage (Volts)
	VO	0	W	0W	Power offset from zero ...
	POWER	PIN		20dBm	Available power of the ...
	FREQ	FLO		920MHz	Frequency (Hz)
	TD	0	s	0s	Delay to start of sine w...
	ALPHA	0		0	Damping factor (1/sec...
	THETA	0	deg	0deg	Phase delay
	TONE	FLO		920MHz	Frequency (Hz) to use f...

29. Click **OK** to close the **Properties** window. If a window opens to assign the source to analyses, dismiss it for now.
30. To add a second power sinusoidal source to Port 1, click **Add to selected port** to open the **Properties** windowv.
31. Set the **POWER** Value field to **PIN**.

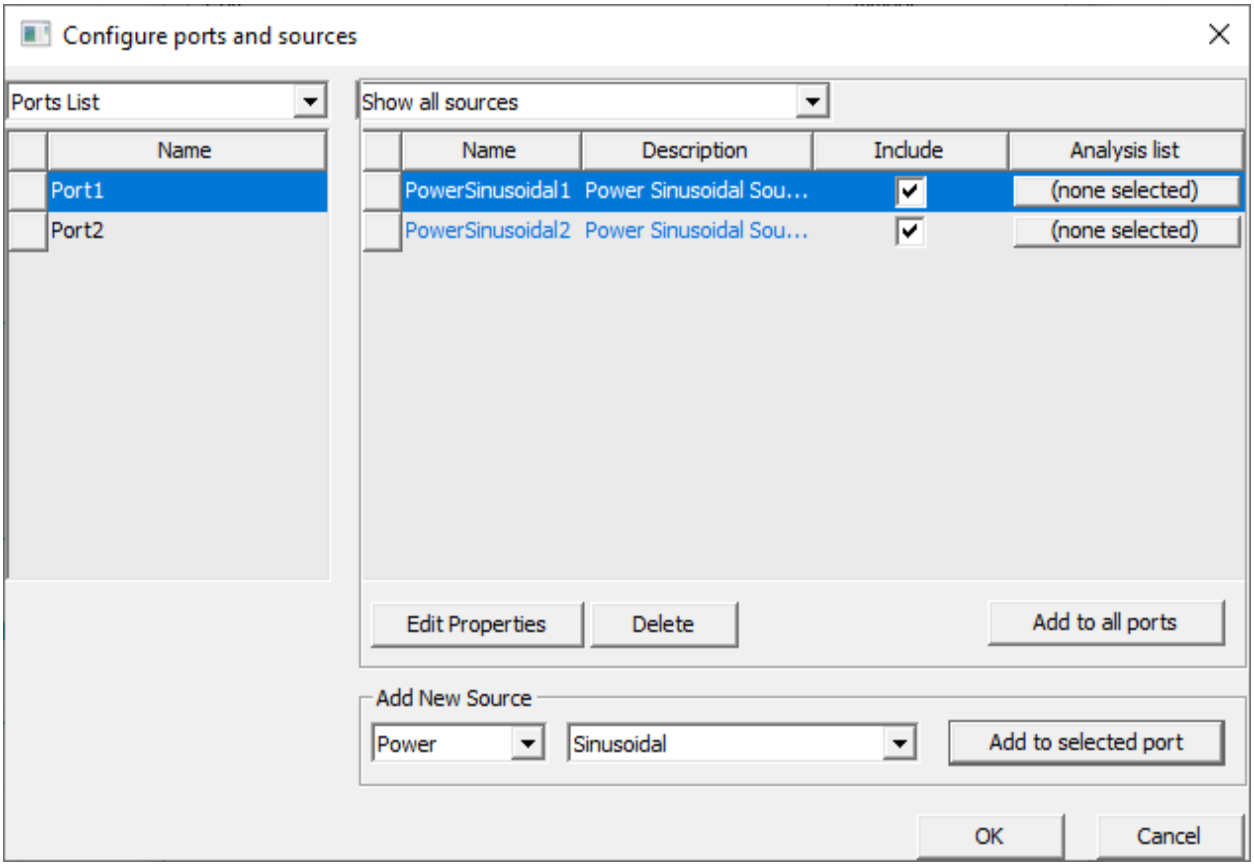
32. Set the **FREQ** Value field to **FRF**. The **Add Variable** window appears:



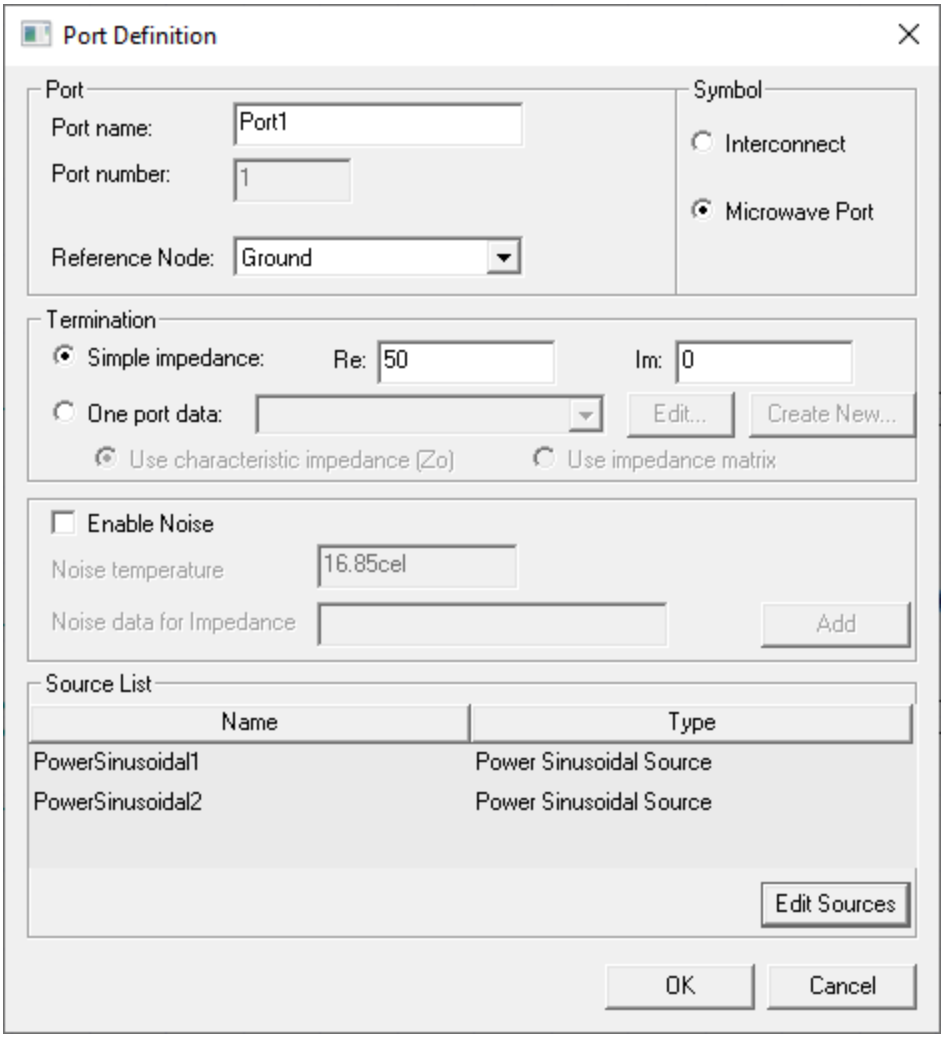
33. Set the **Unit Type** to **Frequency**, the **Unit** to **Hz**, and the **Value** to **970MHz** as shown. Click **OK**.
34. Set the **TONE** Value field to **FRF**. This value is used by harmonic balance. The Parameter Values tab on the **Properties** window for the Power Sinusoidal2 source is shown in the following figure.



35. Click **OK** to close the Properties window. A window opens to assign the source to analyses. Dismiss this window for now.



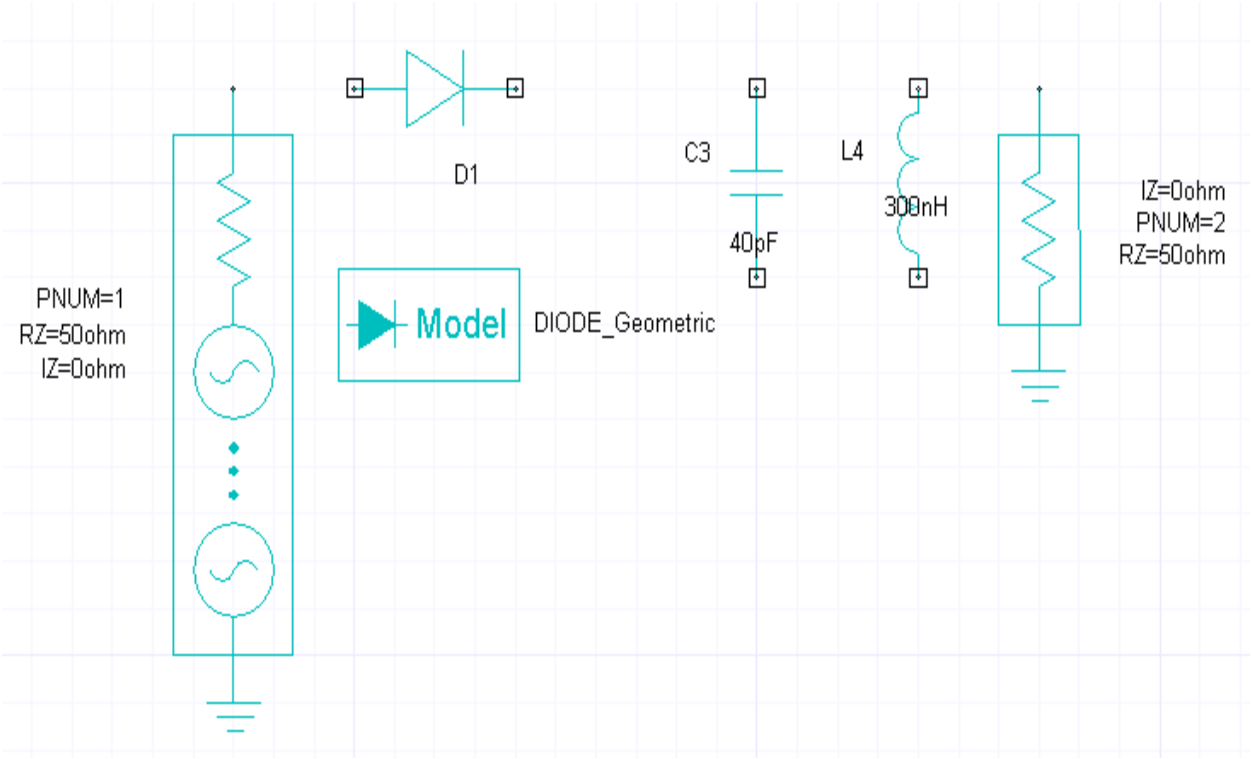
35. Click **OK** to close the **Configure ports and sources** window.



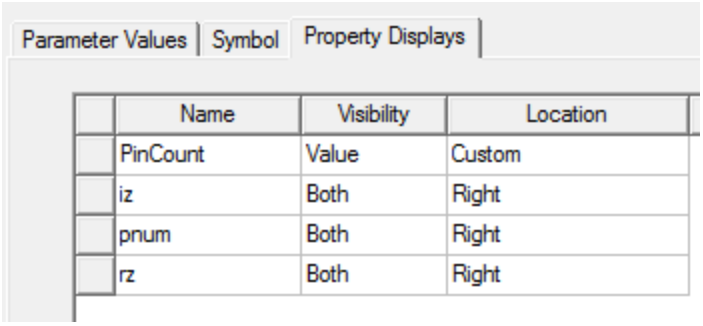
36. Click **OK** to close this window.

37. Double-click Port 2 in the schematic. Select **Microwave port** for the symbol type and click **OK**. Select each of the ports and rotate to point the ground symbol downward.

    The schematic should resemble the following at this point:



38. **Optional:** To relocate the Port 2 property displays as shown above, right-click the symbol and select **Properties**. In the **Properties** window, click the **Property Displays** tab. From the **Location** Value field drop-down menus, select **Right** for the **iz**, **pnum**, and **rz** properties.

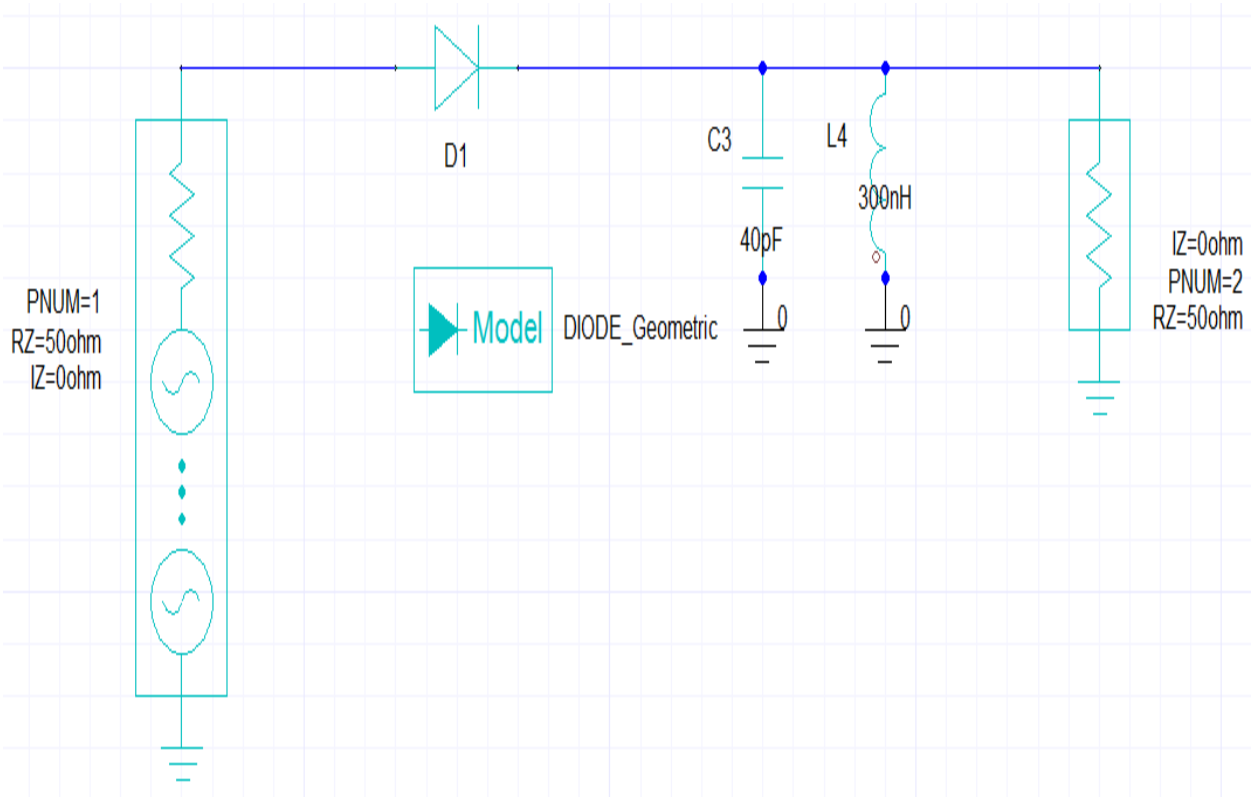


	Name	Visibility	Location
	PinCount	Value	Custom
	iz	Both	Right
	pnum	Both	Right
	rz	Both	Right

39. Click **OK** to close the window.
40. Select the **Ground** icon on the upper-right ribbon are and place grounds on the lower terminals of the capacitor and the inductor components in the design area. The grounds connect to the terminals automatically.

40. Click the output terminal on Port1 to start a wiring operation. A big X appears and a wire is attached to the cursor. Drag the cursor with the wire and connect Port 1 to the input of the diode. Click again to drop the wire.
41. Connect the output of the diode to the upper terminal of the capacitor.
42. Connect the upper terminal of the capacitor to the upper terminal of the inductor.
43. Connect the upper terminal of the inductor to Port 2.

    The schematic should resemble the following picture.



44. Click the **Electronics Desktop File** drop-down menu and select **Save**. A window opens, allowing you to specify the directory where you want to save your work, and the name for your design (the design is saved with an **.aedt** suffix).

The next step is to set up and run Transient and harmonic balance analyses.

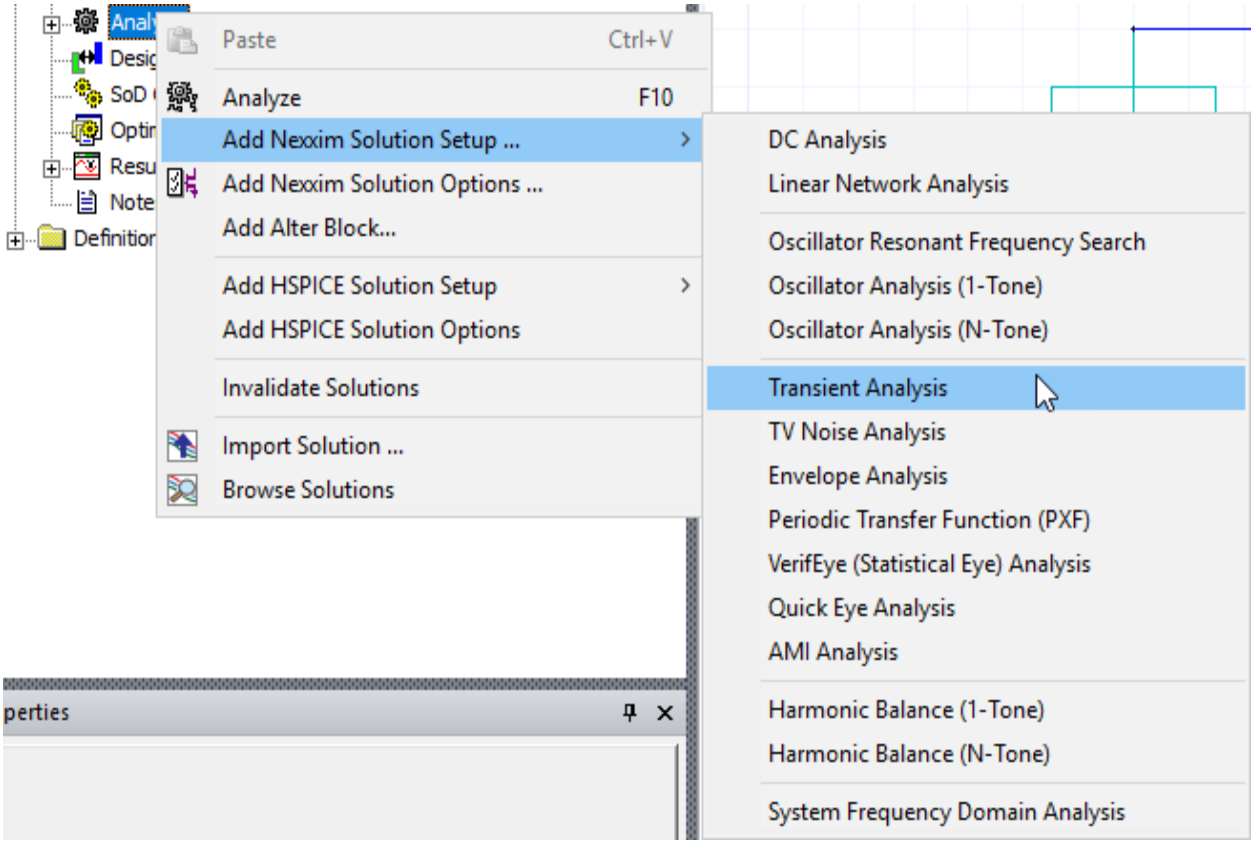
Transient and Harmonic Balance Analyses

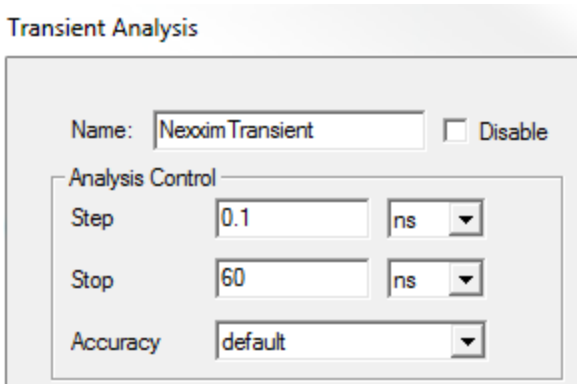
Transient analysis is the time domain simulation of the mixer. You need to run transient only to analyze the start-up period—the first few cycles of the carrier. Harmonic balance analysis reveals the spectral output of the mixer in steady state, and can also provide a time-domain view

of the start-up behavior. After the simulations have been set up, you must assign the two Port 1 power sources to the analyses.

To set up the Transient analysis:

1. In the Project window, expand the **Circuit*n*** folder, right-click the **Analysis** folder, and select **Add Nexxim Solution Setup**. Continue to expand the menu and select **TransientAnalysis** to open the **Transient Analysis** setup window.

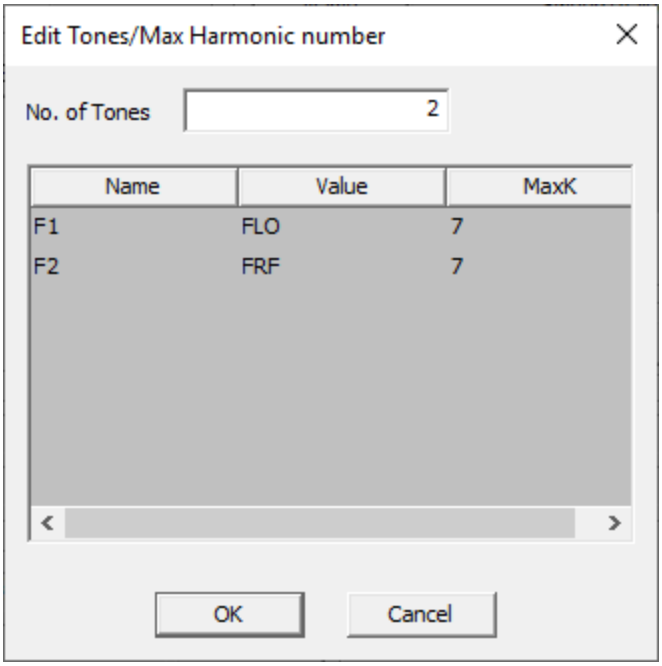




2. Change **Stop** to **60** ns. Step and Accuracy should remain as shown.
3. Click **OK** to close the **Transient Analysis** setup window.

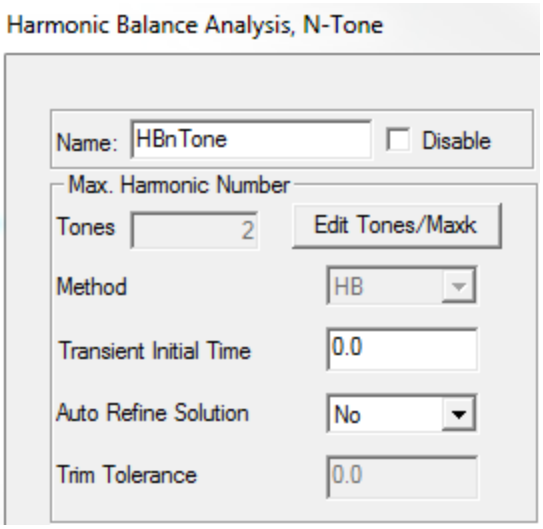
To set up the Harmonic Balance analysis:

1. From the **Project Manager** window, expand the **Project Tree** and [*active design folder*]. Then right-click the **Analysis** folder and select **Add Nexxim Solution Setup** > **Harmonic Balance (N-Tone)** to open the **Harmonic Balance Analysis, N-Tone** window.
2. Click **Edit Tones/max** to open the **Edit Tones/Max Harmonic number** window.



3. Change **No of Tones** to **2**. The group box shows the two tones as F1 and F2.
4. Set the Value of **F1** to **FLO** and the Value of **F2** to **FRF**.

5. Click **OK** to close the **Edit Tones/Max Harmonic number** setup window.

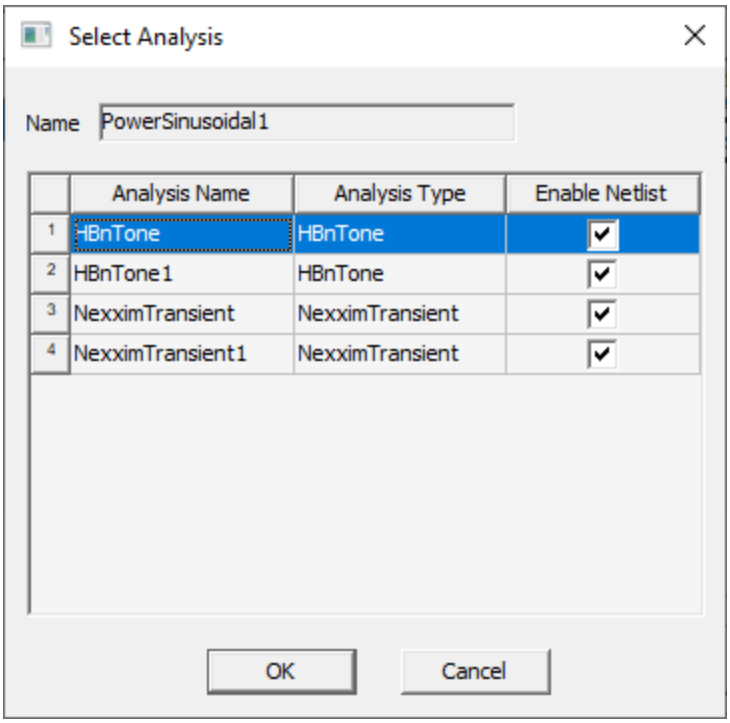


6. Click **OK** to close the **Harmonic Balance Analysis, N-Tone** setup window.

The final step in the set up is to configure the power sinusoidal sources in Port 1 with the analysis setups.

1. Double-click on Port 1 to open the **Port Definition** window.
2. From the **Port Definition** window, select **Edit Sources**.
3. From the **Configure ports and sources** window, click **Select** in the **Analysis List**

column for **PowerSinusoidal1**. The **Select Analysis** window appears:



4. Both analyses are enabled by default. Click **OK** to close the **Select Analysis** window.
5. Click **Select** in the **Analysis List** column for **PowerSinusoidal2**. Verify that this source is also enabled for both analyses.
6. Click **OK** to close the **Configure ports and sources** window.
7. Click **OK** to close the **Port Definition** window.
8. From the **Electronics Desktop File** menu, select **Save**.

Run the Analysis

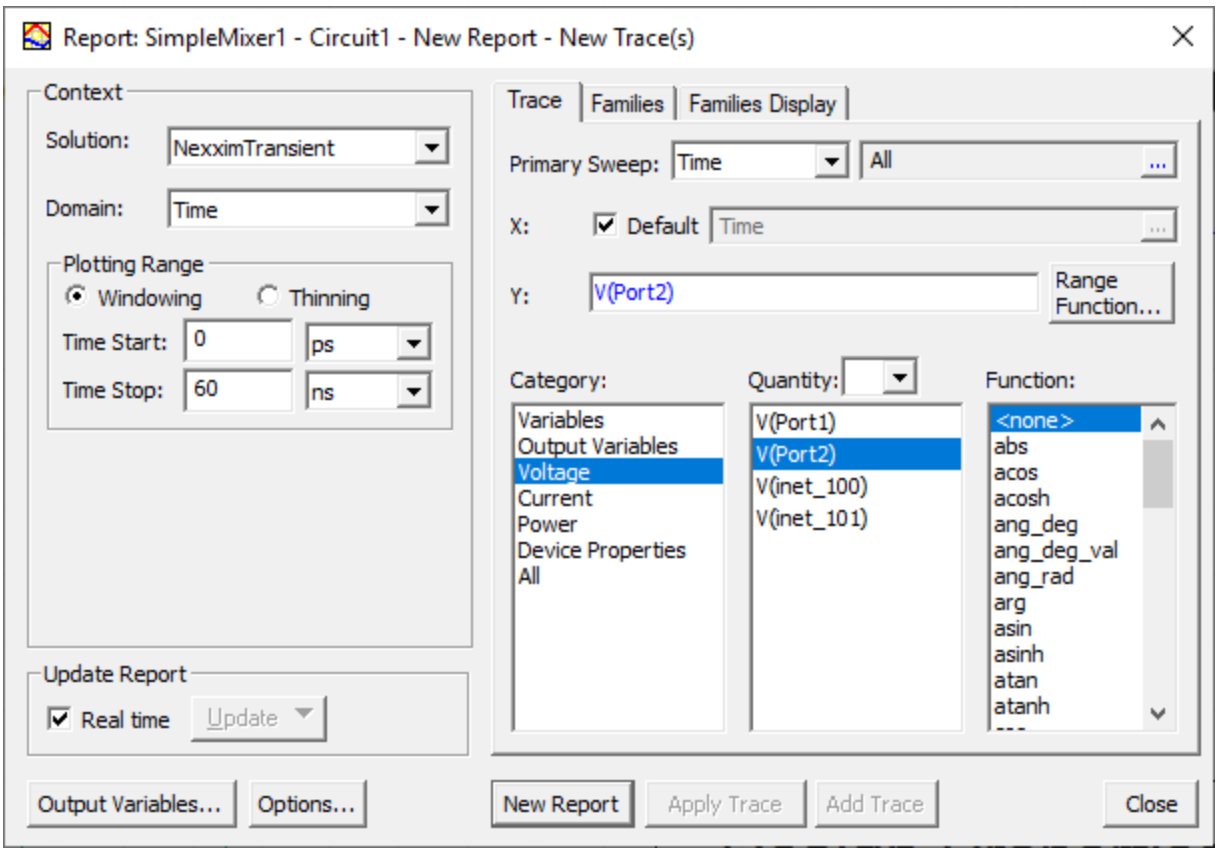
To run both the transient analysis and the harmonic balance analysis, right-click the **Analysis** folder and select **Analyze**. The progress window in the lower-right indicates when the two analyses are being performed. When both analyses are completed, the Message Manager window (lower-center) shows the name of the project, errors or warnings if any, and analysis statistics such as CPU time.

The final step is to display the results of the analyses.

Display the Transient and HB Results

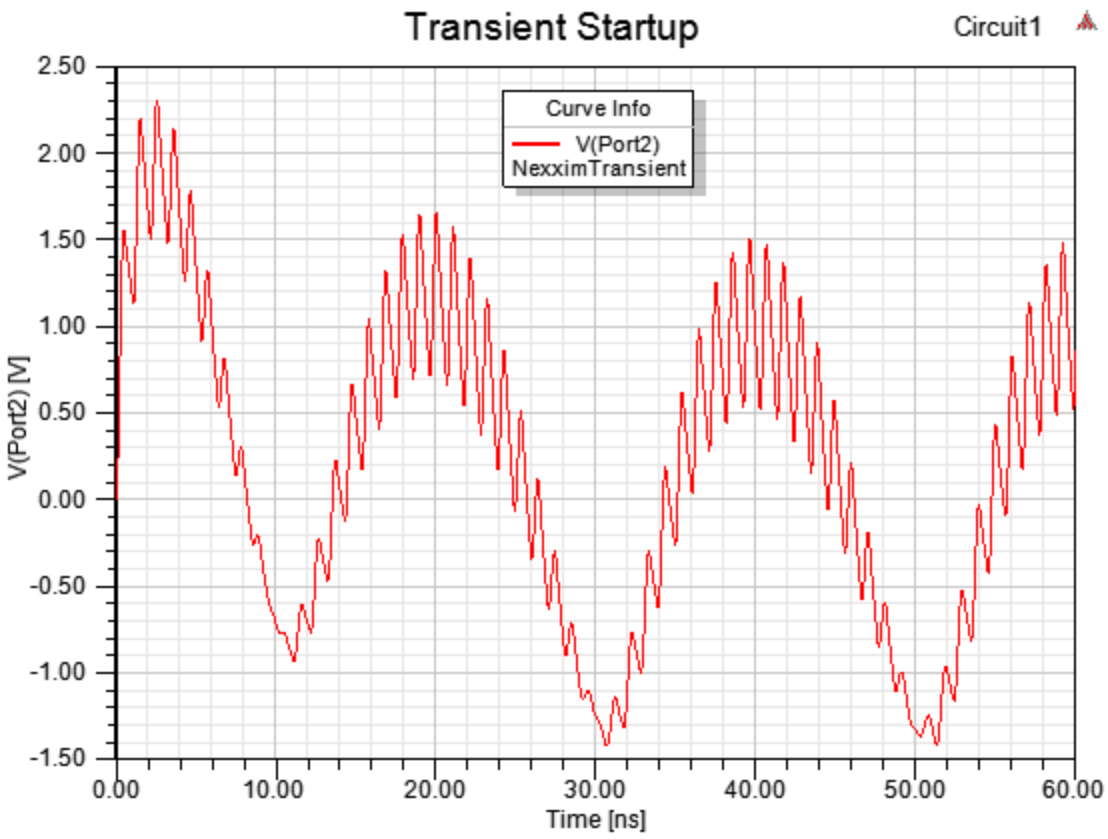
To display the results of the transient analysis:

1. In the **Project Manager** window, right-click the **Results** window and select **Create Standard Report** > **Rectangular Plot** to open the **Report** window.



2.

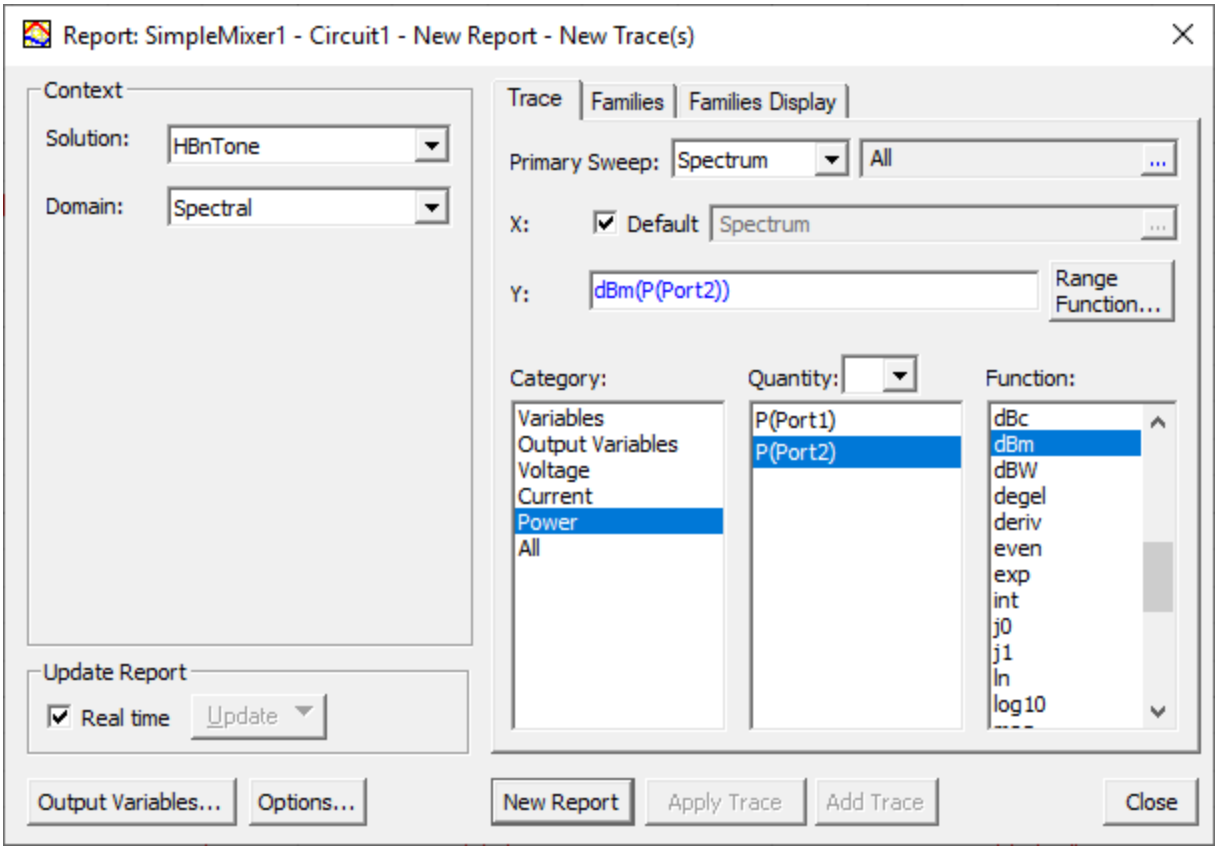
2. The **Context** group box should already have **Nexxim Transient** as the **Solution** and **Time** as the **Domain**.
3. The X-axis (primary sweep) is the time values. For the Y-axis, select the **Voltage** category, the **V(Port2)** quantity, using the **<none> Function** (to report the untransformed real value). Then click **New Report** to open the **Reports** window with the graph of the mixer start-up at output Port 2 in the time domain:



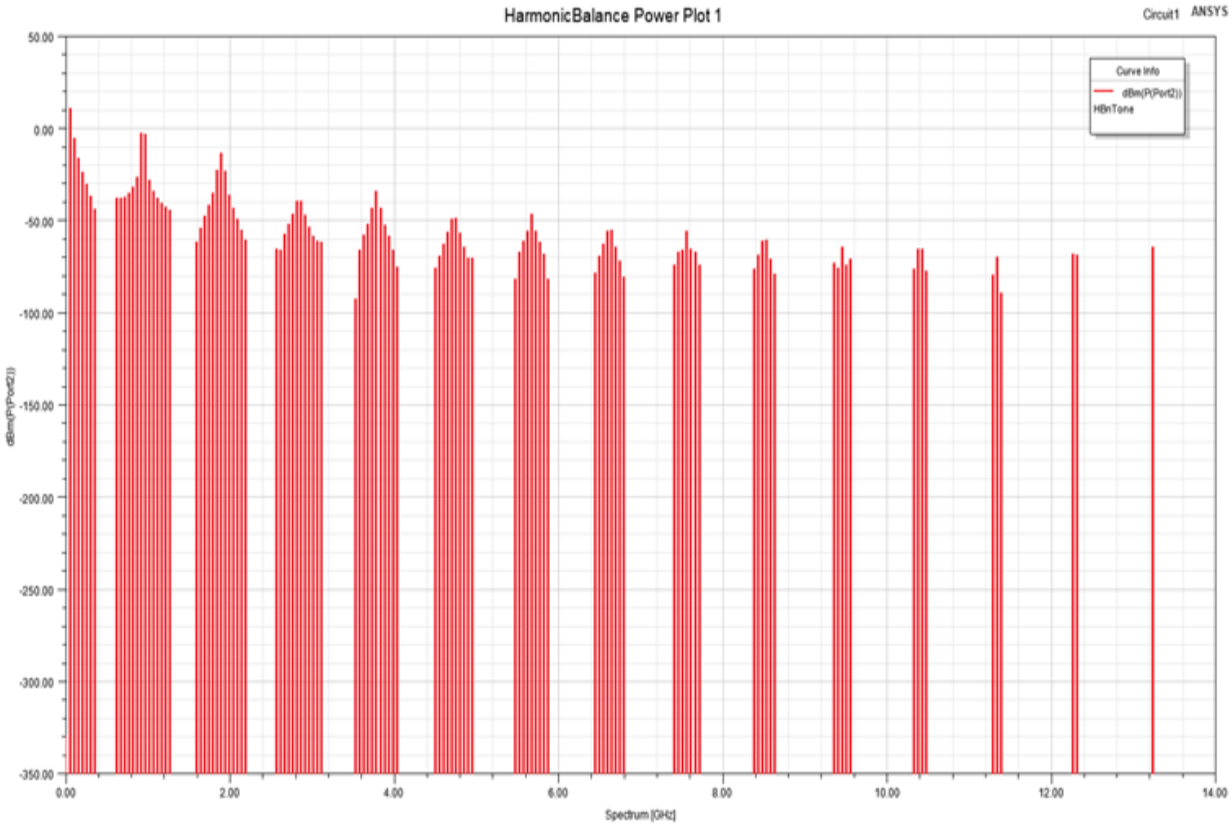
4. Click **Close** to close the **Report** window.
5. Click the **Voltage** icon in the **Results** folder and rename it to **Transient Startup** in the **Properties** window docked in the Project Manager window.

To display the results of the harmonic balance analysis with the steady-state output of the mixer:

1. Click the **Results** icon and select **Create Standard Report** > **Rectangular Plot** to open the **Report** window.



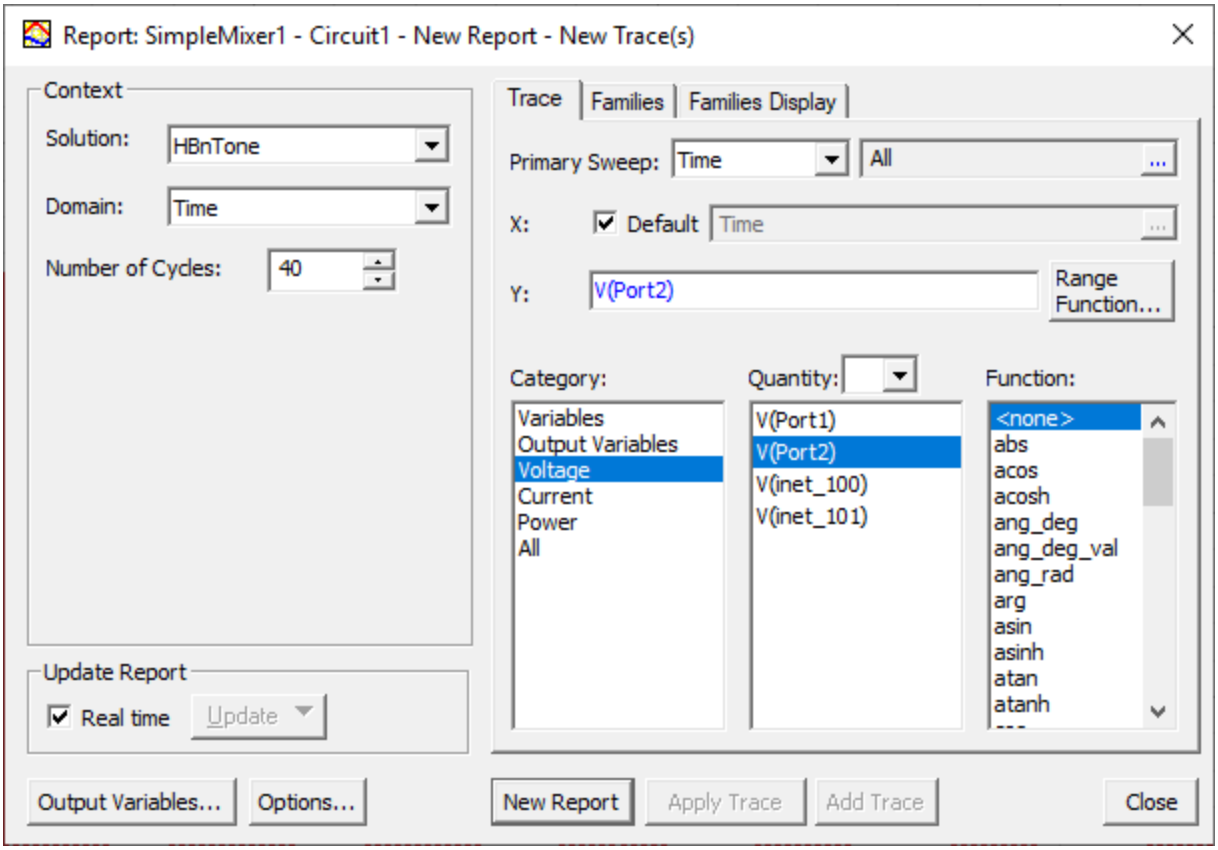
2. Select **HBnTone** as the **Solution** and **Spectral** as the **Domain**.
3. The X-axis (primary sweep) is the frequencies. For the Y-axis, select the **Power** category, the **P(Port2)** quantity, and the **dBm Function** Then click **New Report** to open the **Reports** window with the graph of the mixer steady-state output at Port 2 in the spectral or frequency domain:



4. Click **Close** to close the **Report** window.
5. Click **Power** icon in the Results folder and rename it to **HB Steady State Spectral** in the **Properties** window docked in the **Project Manager** window.

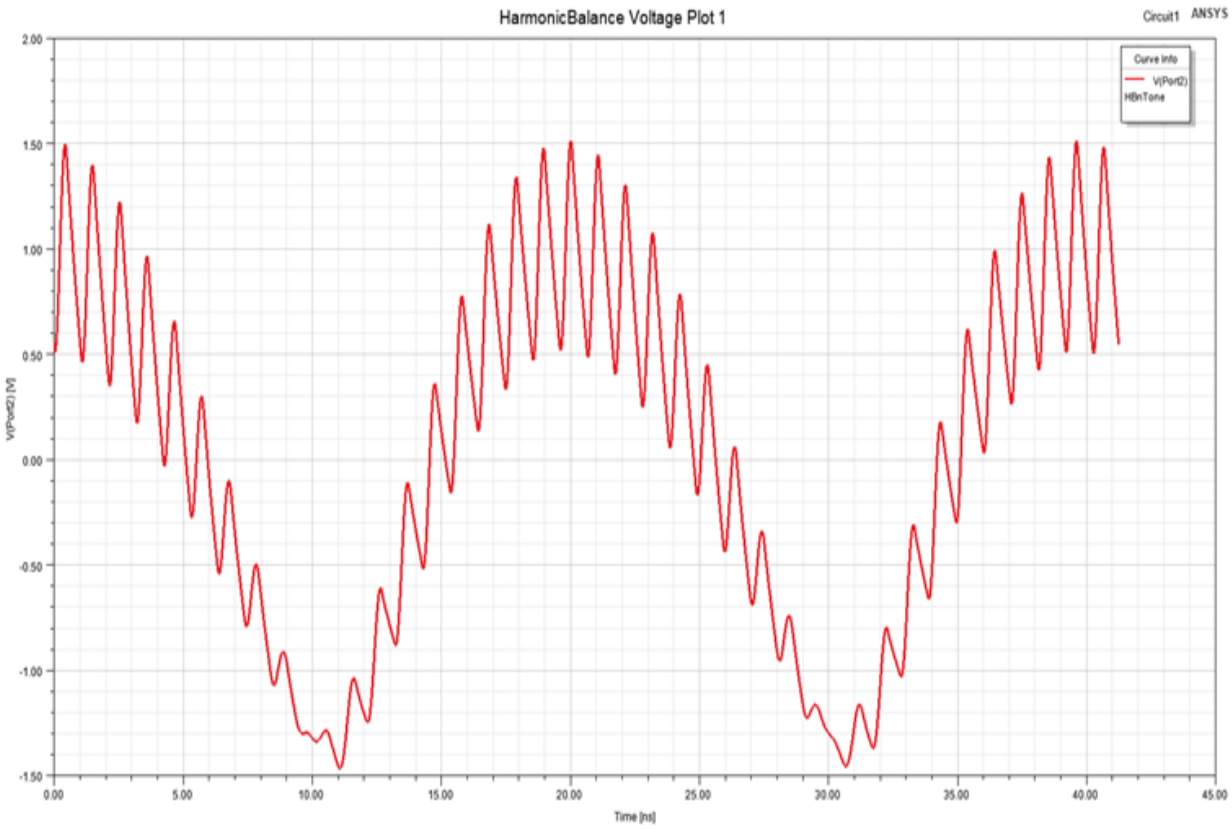
To display the results of the harmonic balance analysis of the output of the mixer at startup, in the time domain:

1. Click the **Results** icon and select **Create Standard Report** > **Rectangular Plot** to open the **Report** window.



2. Select **HBnTone** as the **Solution** and **Time** as the **Domain**.
3. Enter **40** in the **Number of Cycles** field.
4. The X-axis (primary sweep) is the time. For the Y-axis, select the **Voltage** category, the **V (Port2)** quantity, and the **<none> Function**. Then click **New Report**.

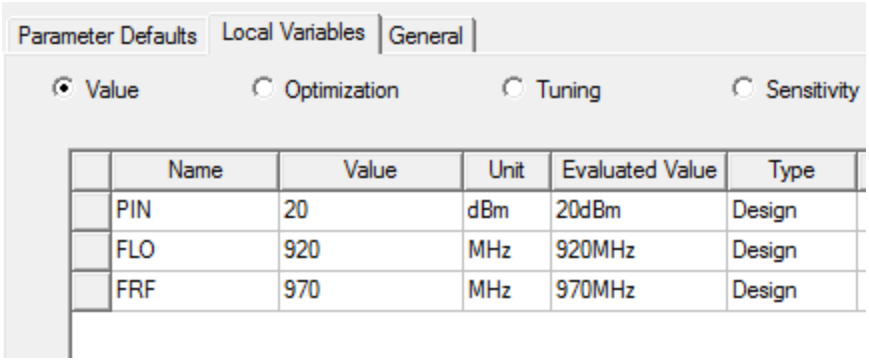
   The **Reports** window opens with the graph of the mixer start-up output at Port 2 in the time domain:



5. Click **Close** to close the **Report** window.
6. Click **Voltage** icon in the Results folder and rename it to **HB Startup Time** in the **Properties** window docked in the **Project Manager** window.
7. Click the **Electronics Desktop File** drop-down menu and select **Save** to save your completed project.

Using the Project Variables

The use of project variables **PIN** for the power input, **FLO** for the carrier frequency, and **FRF** for the signal frequency allows you to easily change these values. To modify the value of a project variable, select the **Circuit** menu at the top of the **Electronics Desktop** window, and click **Design Properties**. Click the **Local Variables** tab:



	Name	Value	Unit	Evaluated Value	Type
	PIN	20	dBm	20dBm	Design
	FLO	920	MHz	920MHz	Design
	FRF	970	MHz	970MHz	Design

Click the **Value** fields to assign new values to the variables.

This concludes the Simple Mixer example.

5 - Simple Channel

This chapter contains the following topics:

Simple Channel Example

This example presents VerifEye and Quick Eye analyses of a piece of a communications channel, a differential transmission line with termination. The expected bit error rate is low, and so a full Transient analysis requires a correspondingly large number of bits. VerifEye estimates the bit error rates based on the statistical parameters of the channel. Quick Eye calculates the impulse response for the channel and applies the waveform to a smaller bit pattern to generate an eye diagram.

As you work through this topic, learn how to:

- Open the example circuit on the Examples directory.
- Alternatively, create the simple channel circuit using the **Schematic Editor**.
- Set up and run VerifEye and Quick Eye analyses.
- Create reports for the results.

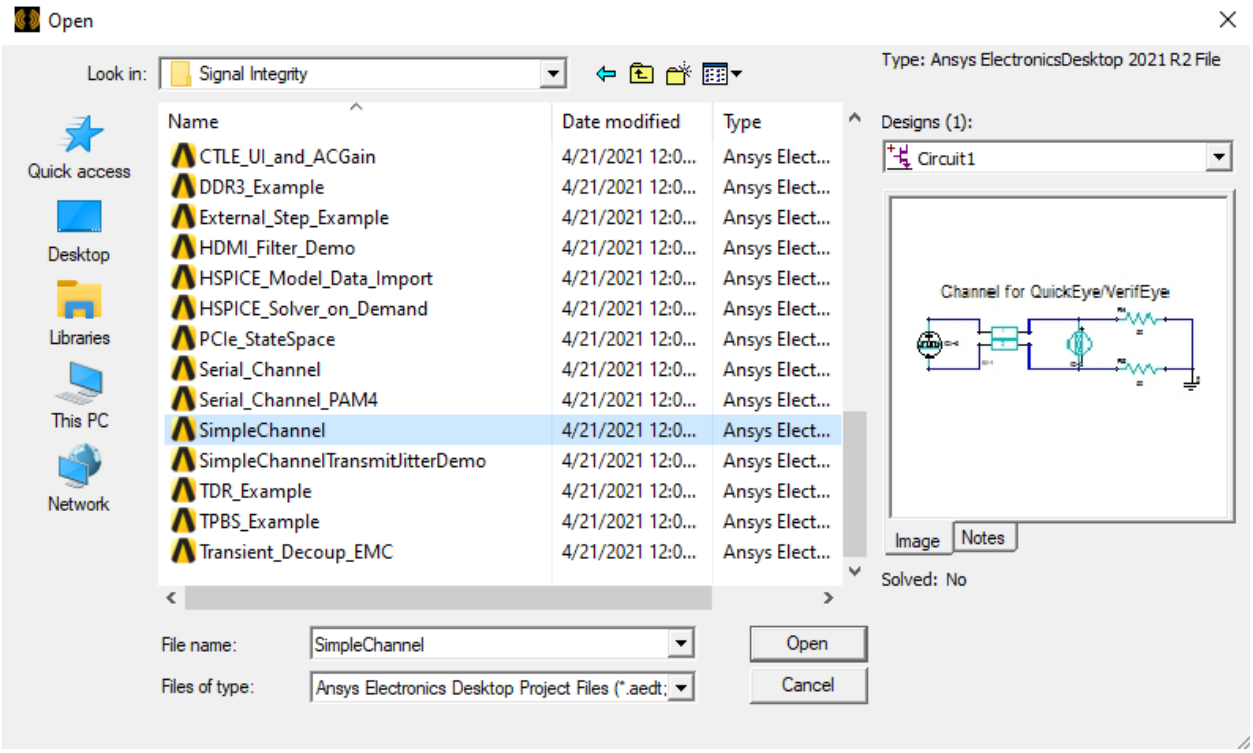
Once the schematic has been set up, you run the simulations and display the results.

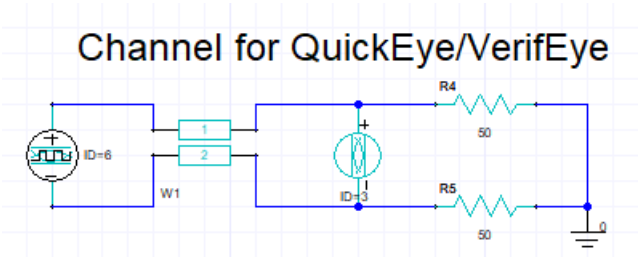
The topics for this example are:

Open the Simple Channel Project on the Examples Directory

Open the simple channel project on the directory of example projects.

1. From the **File** menu, select **Open Examples** to open an explorer window.
2. From the Examples folder, select **Circuit** > **Signal Integrity**. Then double-click **SimpleChannel.aedt**, or select **SimpleChannel.aedt** and click **Open** to open the **Schematic Editor** window to display the mixer schematic.





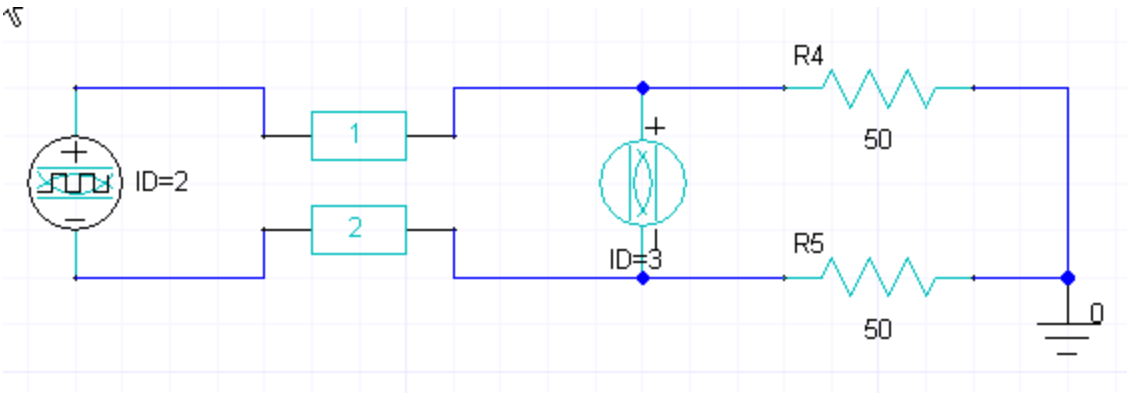
The channel consists of a microstrip differential line and a pair of terminating resistors. The Eye Source on the left specifies the parameters of the input signal including transmitter properties such as transmit jitter and equalization. The Eye source can generate a bit stream for Quick Eye or Transient analysis. The Eye Probe on the right captures the output and can add receiver equalization.

The next step is to set up VerifEye and Quick Eye analyses.

Note: The following topics in this document show how to create this Simple Channel circuit.

Create the Simple Channel with the Schematic Editor

Instead of opening the example on file, use ANSYS Electronics Desktop's **Schematic Editor** to create the channel circuit for simulation. Complete the following steps to create this circuit.

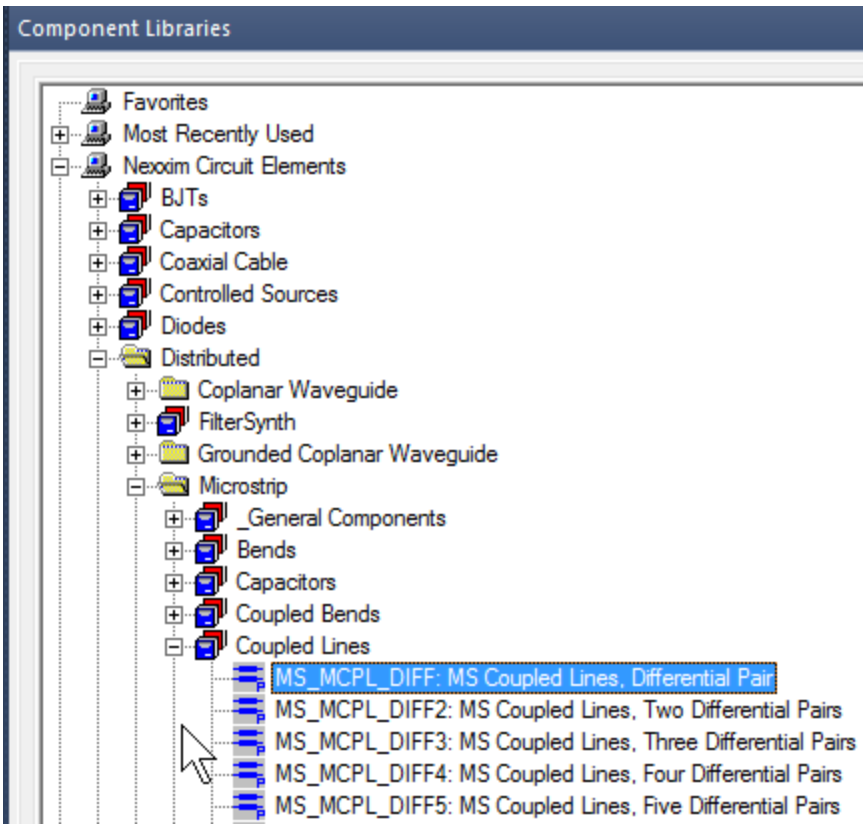


The channel consists of a microstrip differential line and a pair of terminating resistors. The Eye Source on the left specifies the parameters of the input signal including transmitter properties such as transmit jitter and equalization. The Eye source can generate a bit stream for Quick Eye or Transient analysis. The Eye Probe on the right captures the output and can add receiver equalization.

To create the design, follow these steps:

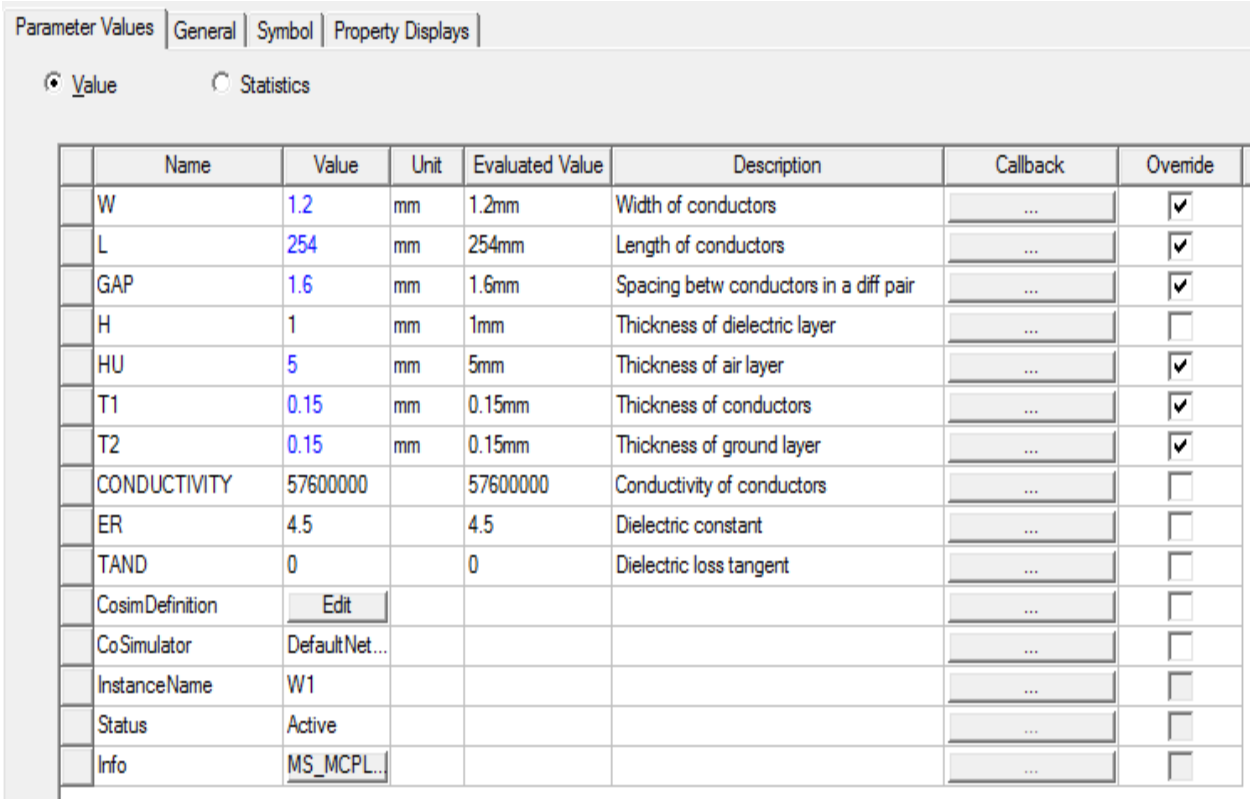
1. Start **Electronics Desktop**. A new project, **Project*n***, should appear (***n*** is the order in which the project was added to the current session of Ansys Electronics Desktop).
2. If no project appears, create one. On the **File** menu, select **New**. A new project named **Project*n*** is added to the **Project Tree**.
3. From the **Project Manager** window, right-click the ***project folder*** and select **Rename**. Our example has been renamed to **SimpleChannel**.
4. From the **Project** menu at the top of the **Electronics Desktop** window, click **Insert Circuit Design** to open the **Choose Technology** window.
5. Click **None**. The microstrip element in our design is a Field Solver component, which generates its own substrate definition.
6. The **Schematic Editor** window opens with an empty design window.

7. Go to the **Component Libraries** window. If you do not see the Component Libraries window, go to **View** and select the **Component Libraries** option. Expand the **Distributed** folder by clicking on the “+" sign. Expand the **Microstrip** folder, then the **Coupled Lines** folder.



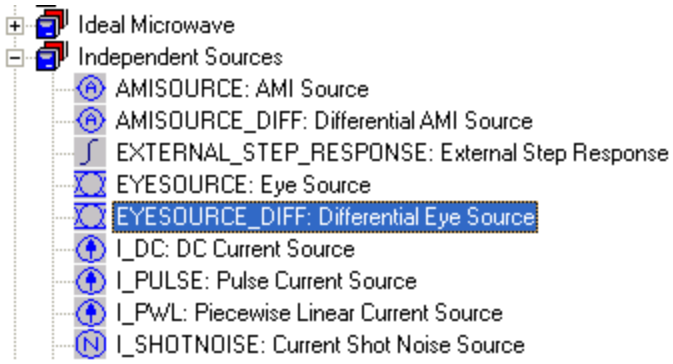
8. Click **MS_MCPL_DIFF:** element, hold down the mouse key and drag the symbol into the design window. Press **Enter** to drop the symbol.

9. Right-click the microstrip element and select **Properties** to open the **Properties** window.



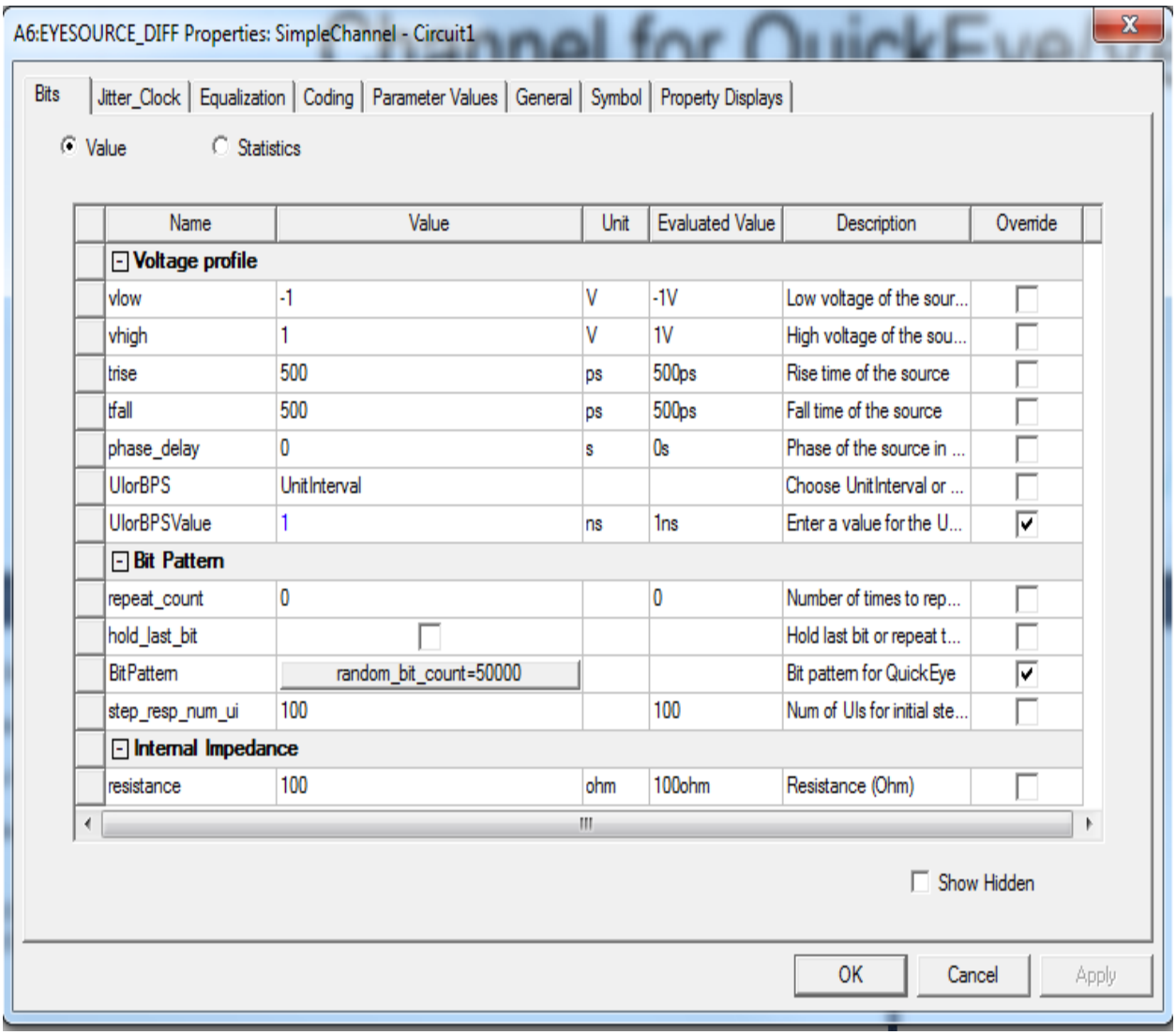
Name	Value	Unit	Evaluated Value	Description	Callback	Override
W	1.2	mm	1.2mm	Width of conductors	...	☑
L	254	mm	254mm	Length of conductors	...	☑
GAP	1.6	mm	1.6mm	Spacing betw conductors in a diff pair	...	☑
H	1	mm	1mm	Thickness of dielectric layer	...	☐
HU	5	mm	5mm	Thickness of air layer	...	☑
T1	0.15	mm	0.15mm	Thickness of conductors	...	☑
T2	0.15	mm	0.15mm	Thickness of ground layer	...	☑
CONDUCTIVITY	57600000		57600000	Conductivity of conductors	...	☐
ER	4.5		4.5	Dielectric constant	...	☐
TAND	0		0	Dielectric loss tangent	...	☐
CosimDefinition	Edit				...	☐
CoSimulator	DefaultNet...				...	☐
InstanceName	W1				...	☐
Status	Active				...	☐
Info	MS_MCPL...				...	☐

10. Set **W** to 2mm, **L** to 254mm, **GAP** to 1.6mm, **HU** to 5mm, **T1** and **T2** both to 0.15mm, as shown above. Leave **H**, **CONDUCTIVITY**, **ER**, and **TAND** at their default values.
11. From the **Components** tab, expand the **Independent Sources** folder.



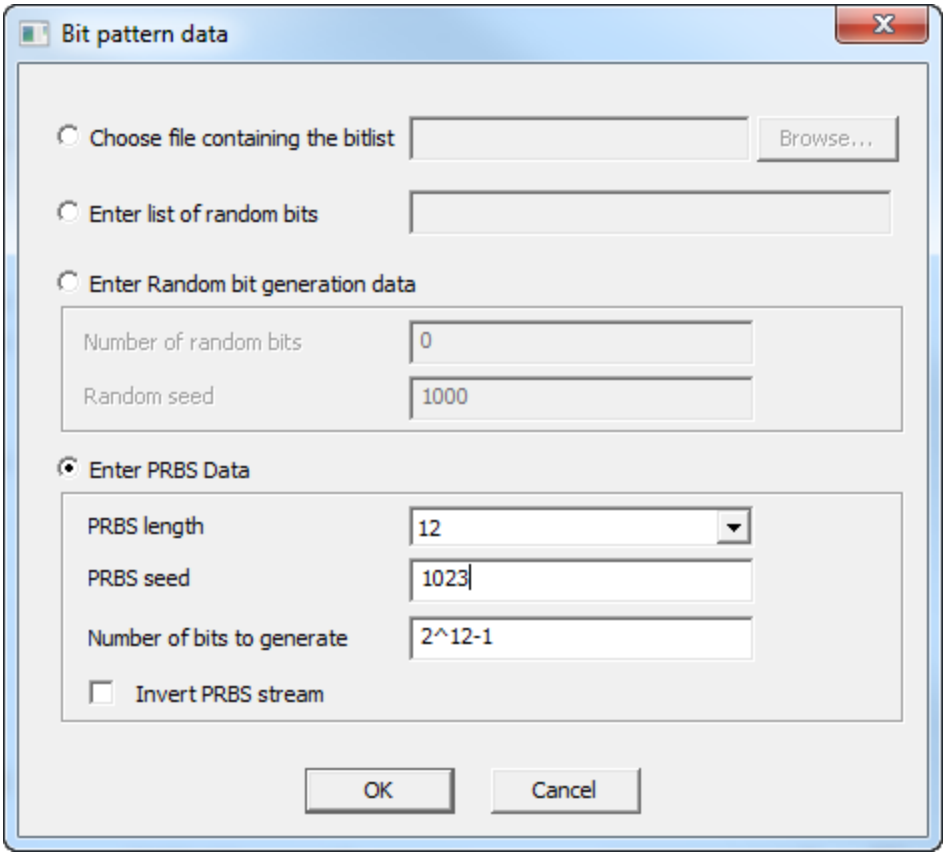
12. Click **EYESOURCE_DIFF:** element, hold down the mouse key and drag the symbol into the design window, at the left of the MS element. Press **Enter** to drop the symbol.

13. Right-click the Eye Source and select **Properties** to open the **Properties** window to the **Bits** tab



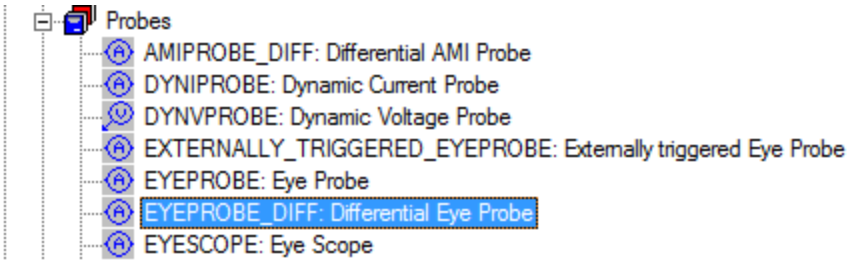
14. Set the Eye Source for a Unit Interval of 1ns, equivalent to a bit rate of 1 GHz/s. The rise and fall times are both 0.5ns.

15. Click in the **BitPattern** Value field. The **Bit pattern data** window opens:

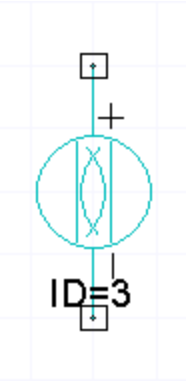


16. Select **Enter PRBS Data**. Select 12 as the **PRBS length** and 1023 as the **PRBS seed**. This sets up a pseudo-random bit stream for Quick Eye. Click **OK** to close the **Bit pattern data** window. The **BitPattern** Value field shows the PRBS setup.

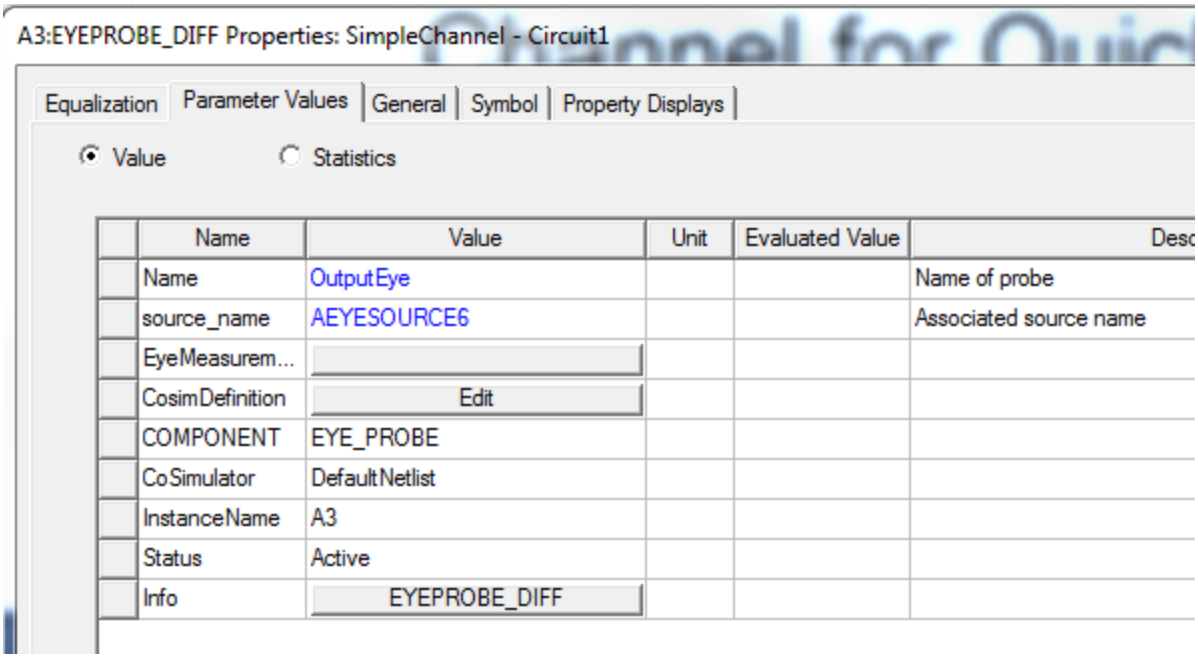
17. Click **OK** to close the Eye Source **Properties** window.
18. From the **Components** tab, expand the **Probes** folder



19. Click the **EYEPROBE_DIFF:** element, hold down the mouse key and drag the symbol into the design window to the right of the MS element. Press **Enter** to drop the symbol.
20. Select the Eye Probe and press **Ctrl** +**R** three times to rotate the symbol so it is vertical with its *positive terminal upward:*



21. Right-click the Eye Probe and select **Properties** to open the **Properties** window. Select the **Parameter Values** tab:



22. Set the **Name** property to **OutputEye** (or other unique name). This property allows for multiple Eye Probes.
23. Click **OK** to close the Eye Source Properties window.
24. From the Components group box, expand the **Resistors** folder. Select the **RES_:** element, drag and place two resistors at the right of the Eye Probe, lining up with the

upper and lower terminals of the probe. The default resistance of 50 ohm should be fine for this circuit.

25. Select the **Ground** icon on the upper-right ribbon area.
26. Click the positive terminal of the Eye Source to start a wire operation. A big X appears and a wire is attached to the cursor. Drag the cursor with the wire to the positive (upper) input terminal of the MS transmission line. Click again to drop the wire. Connect the negative terminal of the source to the lower input of the MS transmission line.
27. Connect the positive (upper) output of the MS line to the positive terminal of the Eye Probe. Connect the lower output of the MS transmission line to the negative terminal of the Eye Probe.
28. Connect the upper terminal of the Eye Probe to the upper resistor. Connect the lower terminal of the Eye Probe to the lower resistor.
29. Connect the two resistor outputs to the ground symbol. The schematic should look like the example given at the beginning of the topic. See the figure "" on page 5-2
30. From the **Electronics Desktop File** menu, select **Save to save the project**.

The next step is to set up and run VerifEye and Quick Eye analyses.

Set Up VerifEye and Quick Eye Analyses

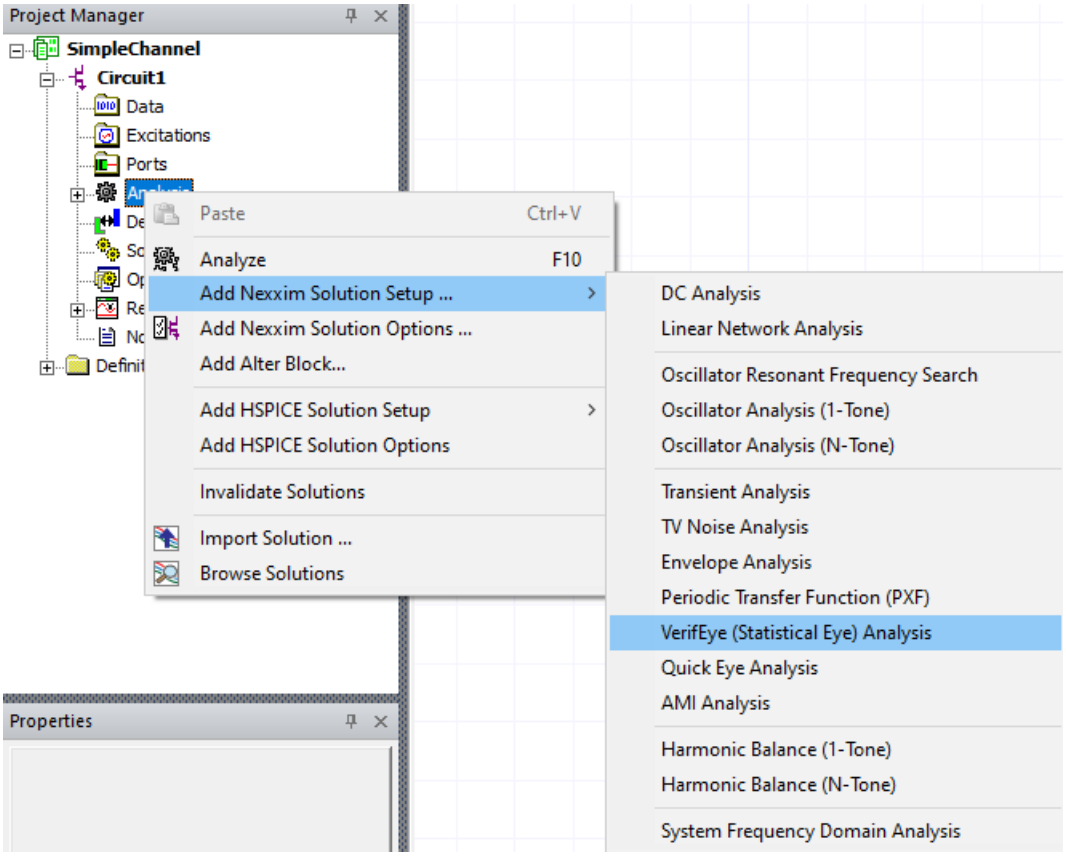
Complete the following steps to set up the VerifEye and Quick Eye analyses.

Set Up VerifEye Analysis

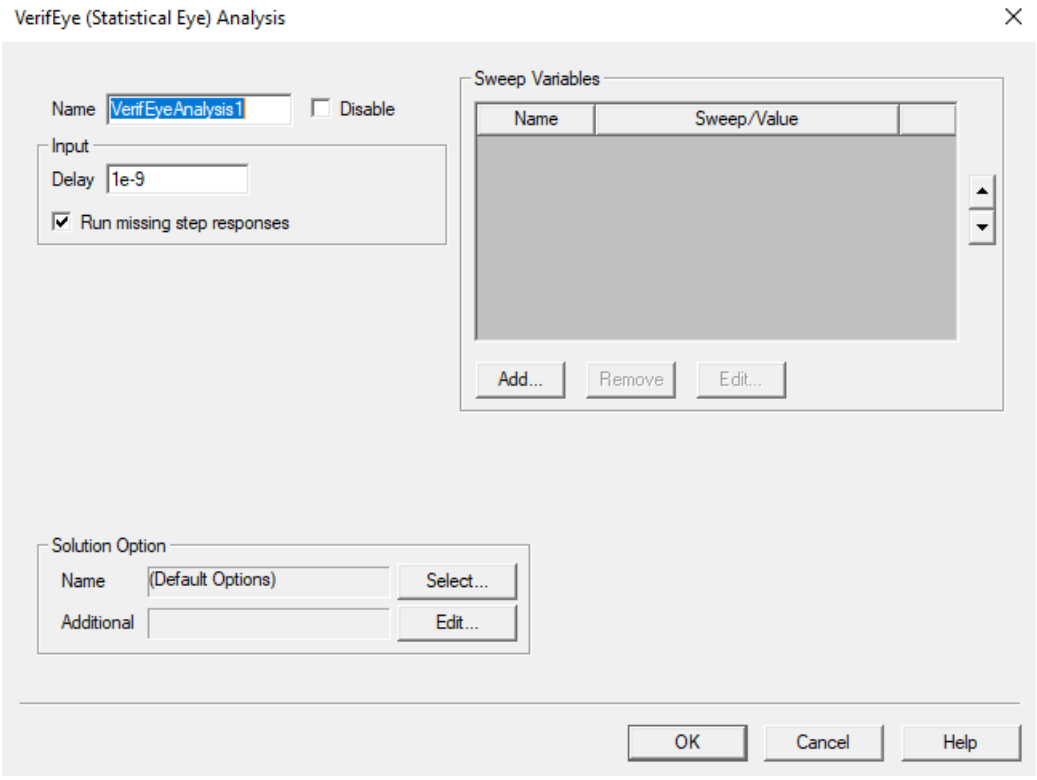
Complete the following steps to set up the VerifEye analysis.

1. From the **Project Manager** window, expand the **Project Tree** and [*active design folder*]. Then right-click the **Analysis** folder and select **Add Nexxim Solution Setup ...** > **VerifEye (Statistical Eye) Analysis** to open the **VerifEye (Statistical Eye) Analysis**

window.



4. All the properties remain as shown. Click **OK** to close the **VerifEye (Statistical Eye) Analysis** window.

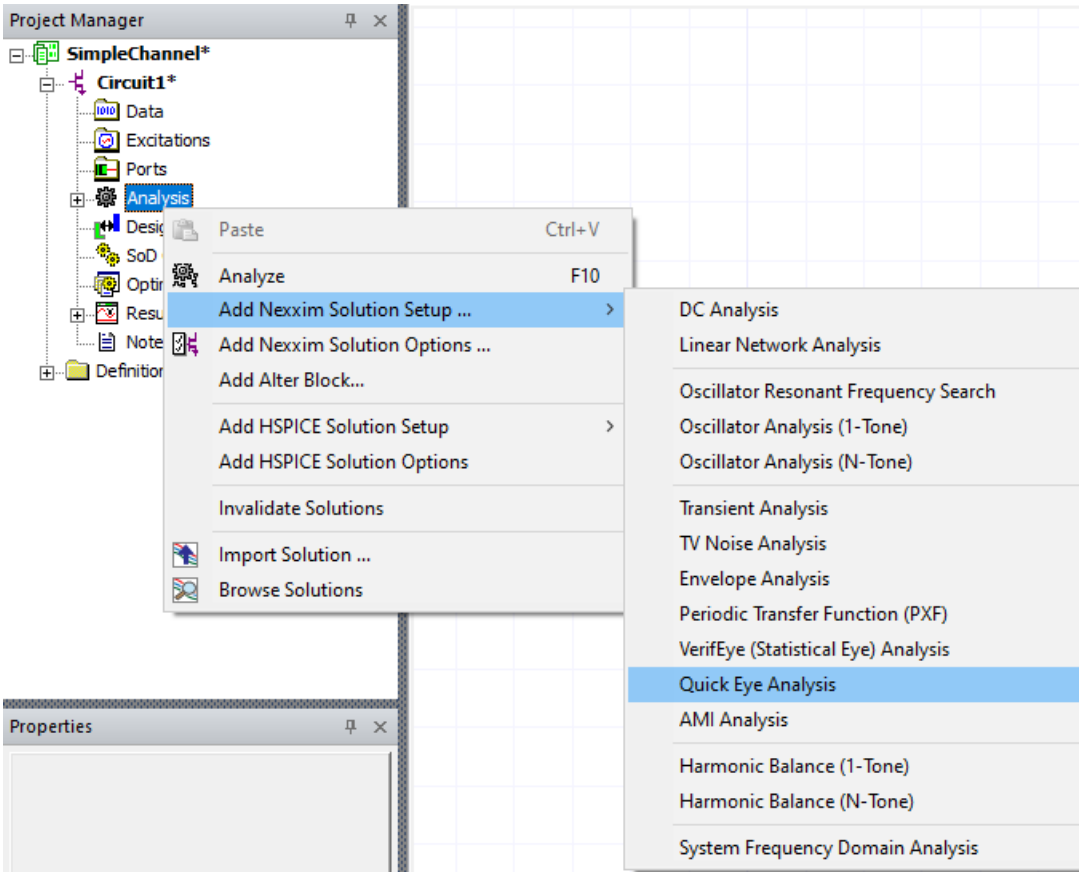


Set Up Quick Eye Analysis

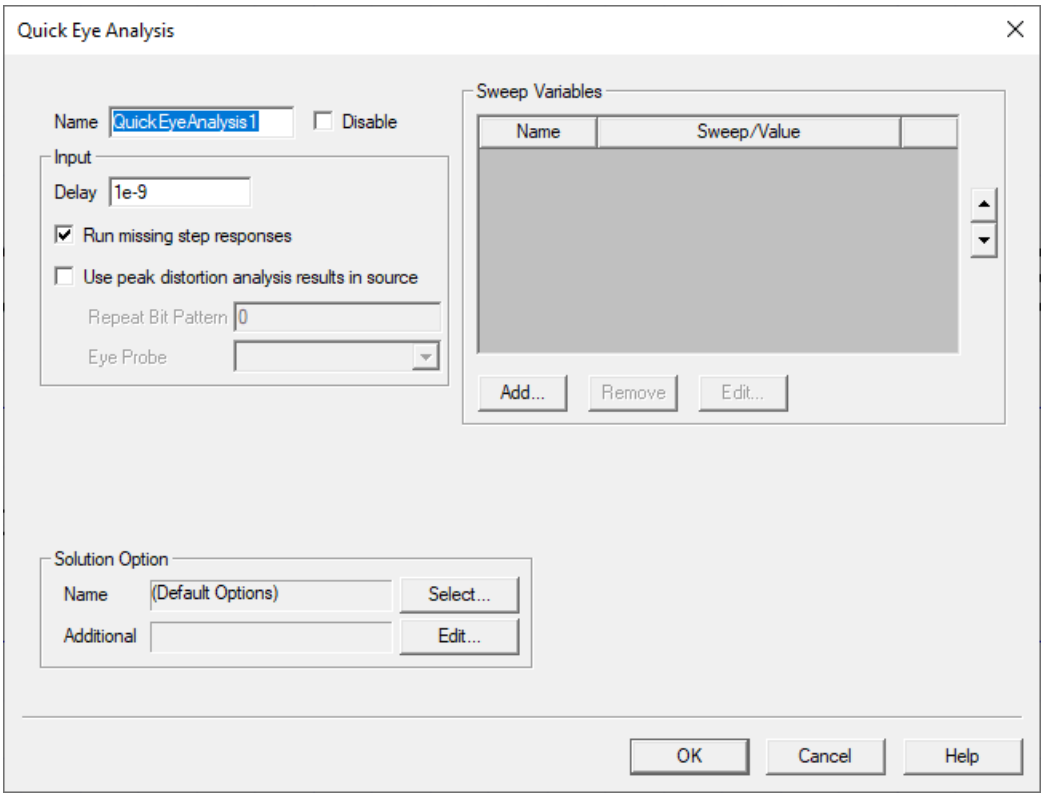
Complete the following steps to set up the Quick Eye analysis.

1. From the **Project Manager** window, right-click the **Analysis** folder and select **Add Nexxim Solution Setup ...** > **Quick Eye Analysis** to open the **Quick Eye Analysis**

window.



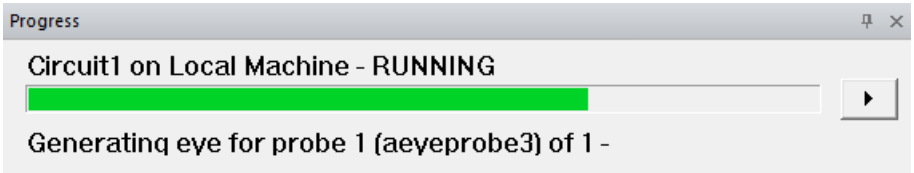
2. All the properties remain as shown. Click **OK** to close the **QuickEye Analysis** window.



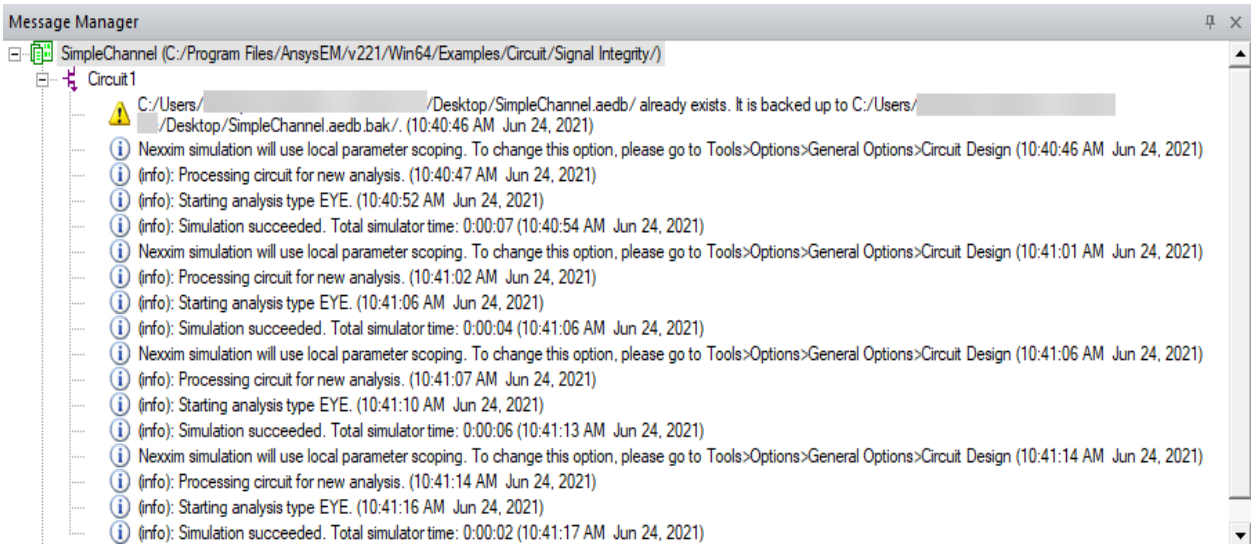
The next step is to run VerifEye and Quick Eye analyses simultaneously.

Run the VerifEye and Quick Eye Analyses

To run both VerifEye and Quick Eye analyses simultaneously, on the **Project Manager** window, right-click the **Analysis** folder under the Project Tree and select **Analyze**. The Progress window indicates when the two analyses are being performed.



When the analyses complete, the Message Manager window at the lower left shows the name of the project, errors or warnings (if any), and analysis statistics (e.g., CPU time).



The next step is to display the results of the analyses and rename the reports.

Display VerifEye/Quick Eye Results and (Optionally) Rename a Report

These instructions explain how to display and rename four report types that are common in signal integrity (SI) studies: a bathtub plot and a contour diagram to display the results of VerifEye analysis, and a bathtub plot to display Quick Eye (QE) analysis results.

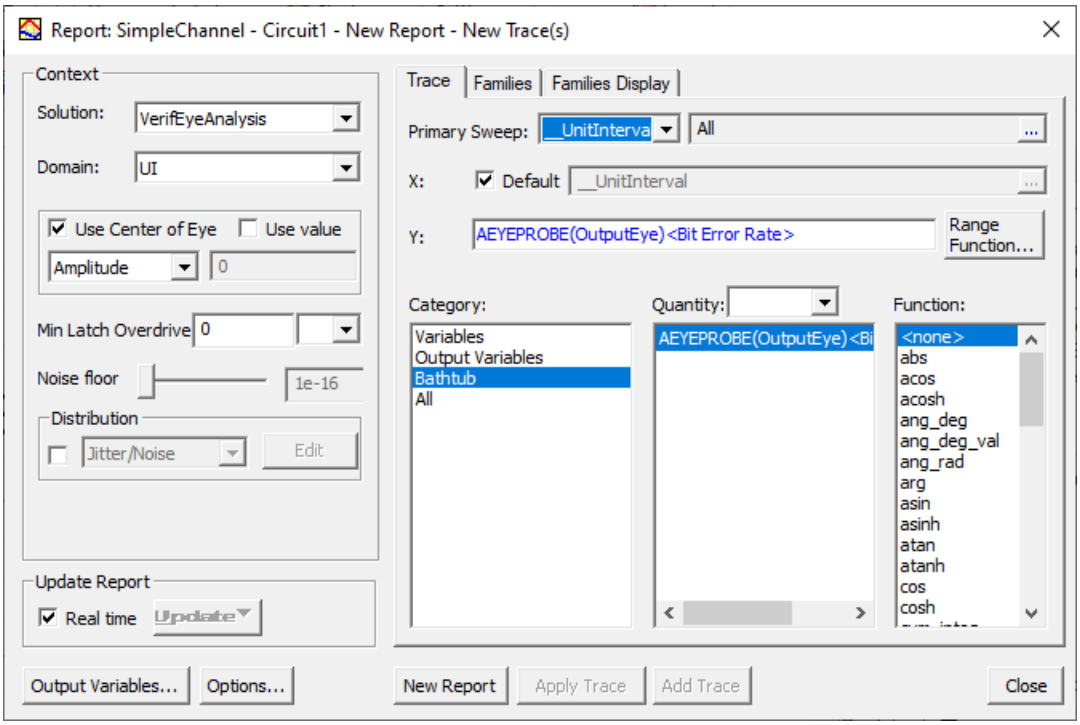
> **Note:** If bathtub curves are plotted and txrj is present, if the number of bits is less than 2.5e5, QE plots present a warning message. Distinguish simulated and extrapolated regions with a partitioning horizontal line using the 'SimulatedLimit' option that is in the 'Quantity' column.

Display a Bathtub Plot of the VerifEye Analysis

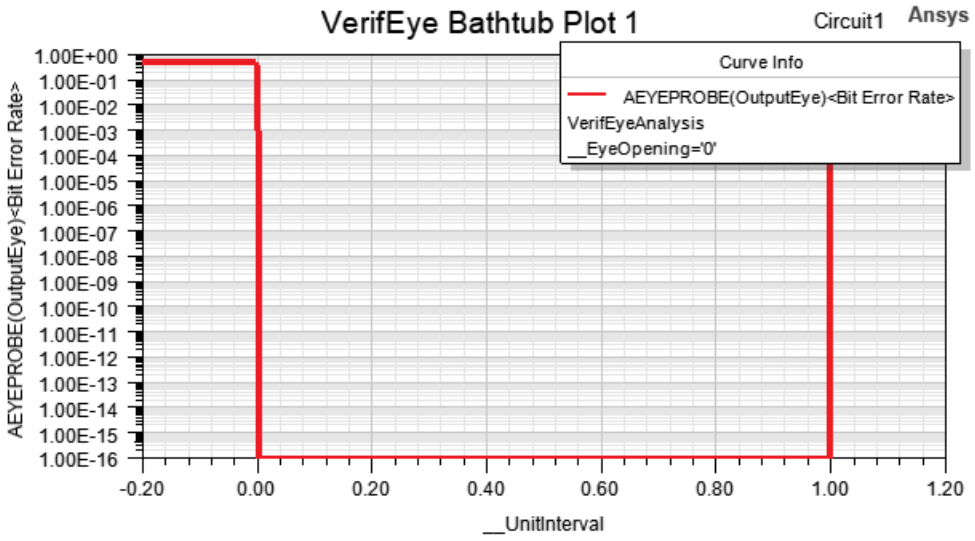
Complete the following steps to display a bathtub plot of the VerifEye analysis.

1. From the **Project Manager** window, expand the **Project Tree** and [*active design folder*]. Then right-click the **Results** folder and select **Create Standard Report** > **Rectangular**

Plot to open the **Report** window.



2. From the **Context** group box, ensure that the **Solution** selection is **VerifEyeAnalysis** and the **Domain** selection is **UI**. These are the default settings.
3. From the **Trace** tab, ensure that the **Primary Sweep** selection is **_UnitInterval**, the **Category** selection is **Bathtub**, the **Quantity** selection is **AEYEPROBE(OutputEye)**, and **<none>** is the **Function** selection. These are the default settings.
4. Click **New Report** to open the **"VerifEye Bathtub Plot 1"** in the **View** tab. The graph shows the bit error rates calculated by VerifEye over the Unit Interval.

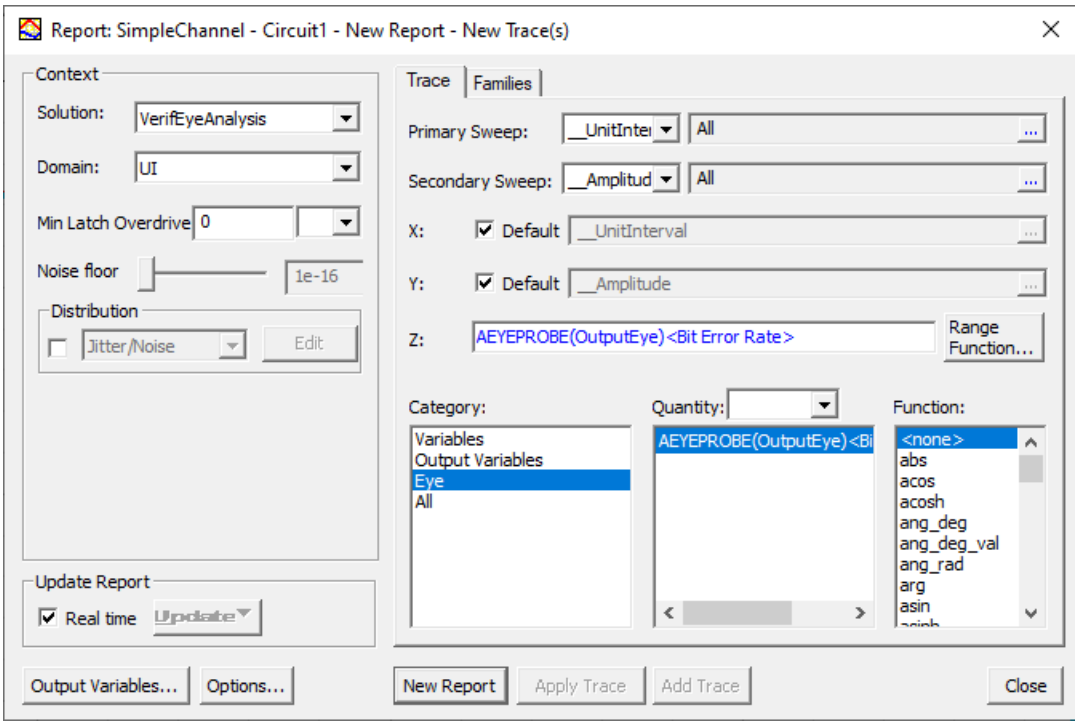


4. Click **Close** to close the **Report** window.

Display a Contour Plot of the VerifEye Analysis

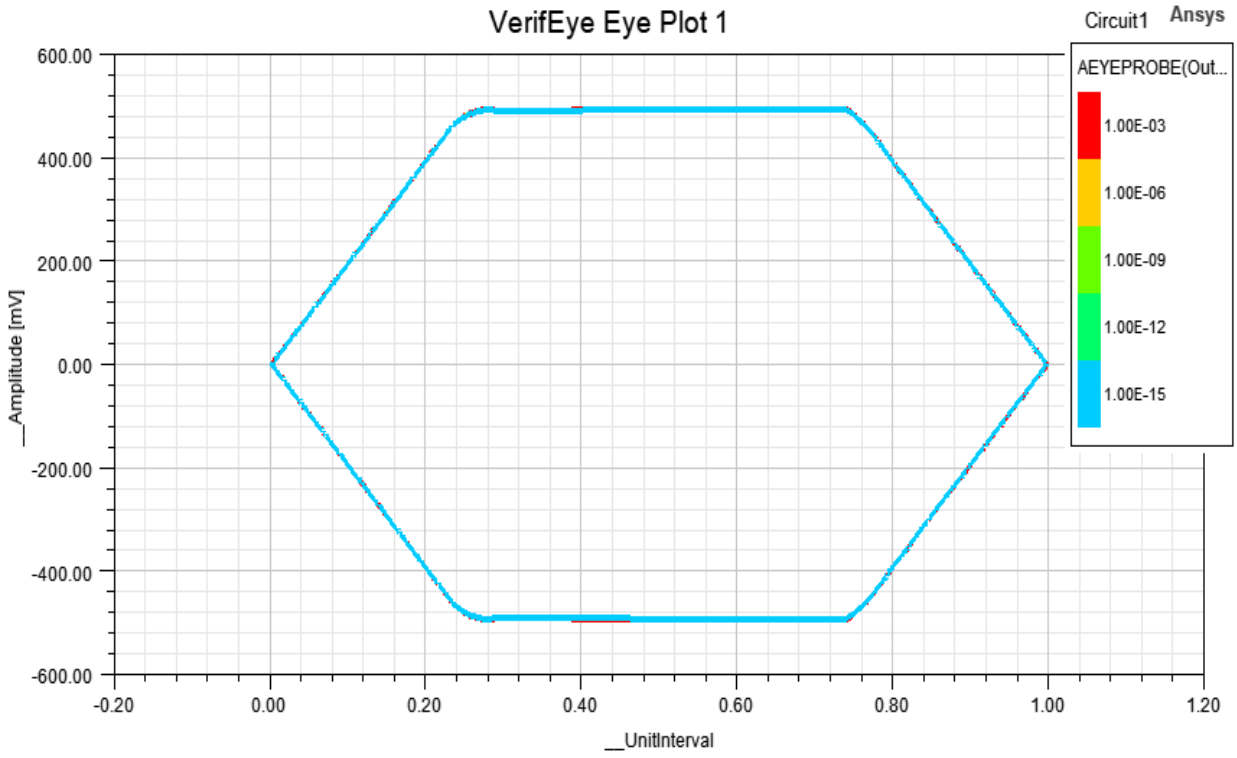
Complete the following steps to display a contour plot of the VerifEye analysis.

1. If necessary, on the **Project Manager** window, expand the **Project Tree** and [*active design folder*]. Then right-click the **Results** folder and select **Create Standard Report** > **Rectangular Contour Plot** to open the **Report** window.



2. From the **Context** group box, ensure that the **Solution** selection is **VerifEyeAnalysis** and the **Domain** selection is **UI**. These are the default settings.
3. From the **Trace** tab, ensure that the **Primary Sweep** selection is **_UnitInterval**, the **"Z-axis"** selection is **AEYEPROBE(OutputEye)<Bit Error Rate>**, the **Category** selection is **Bathtub**, the **Quantity** selection is **AEYEPROBE(OutputEye)**, and **<none>** is the **Function** selection. These are the default settings.

4. Click **New Report** to open the **"VerifEye Eye Plot 1"** in the **View** tab. The graph shows the bit error rates calculated by VerifEye as a contour diagram.



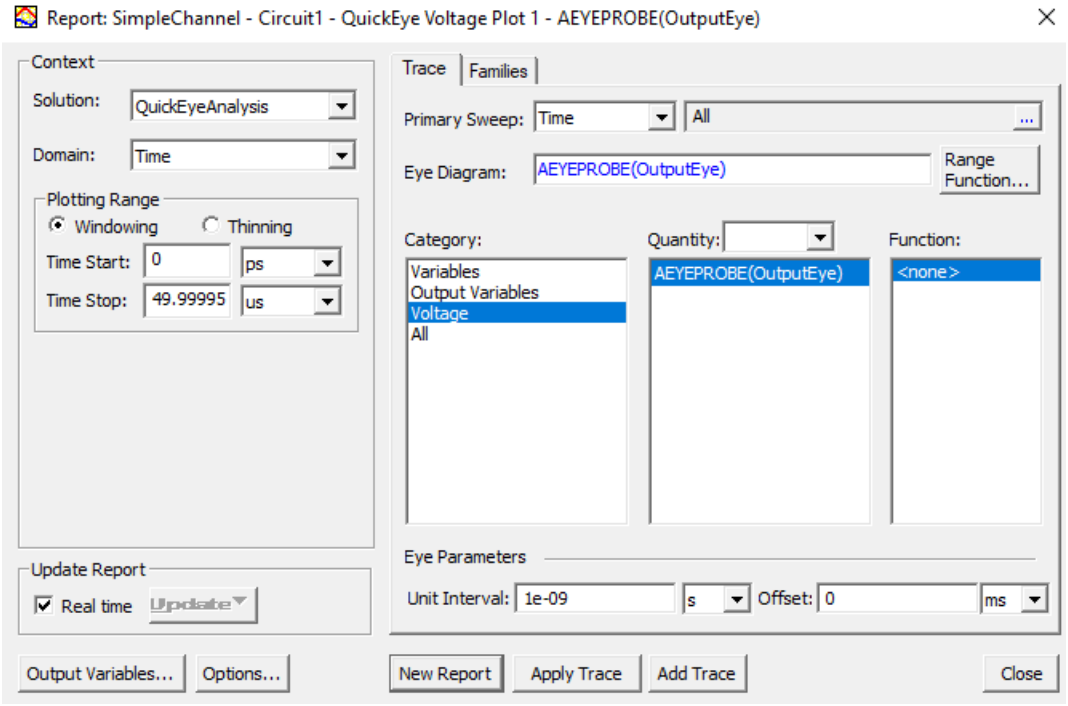
5. Click **Close** to close the **Report** window.

Display an Eye Diagram of the Quick Eye Analysis

Complete the following steps to display an eye diagram of the Quick Eye analysis.

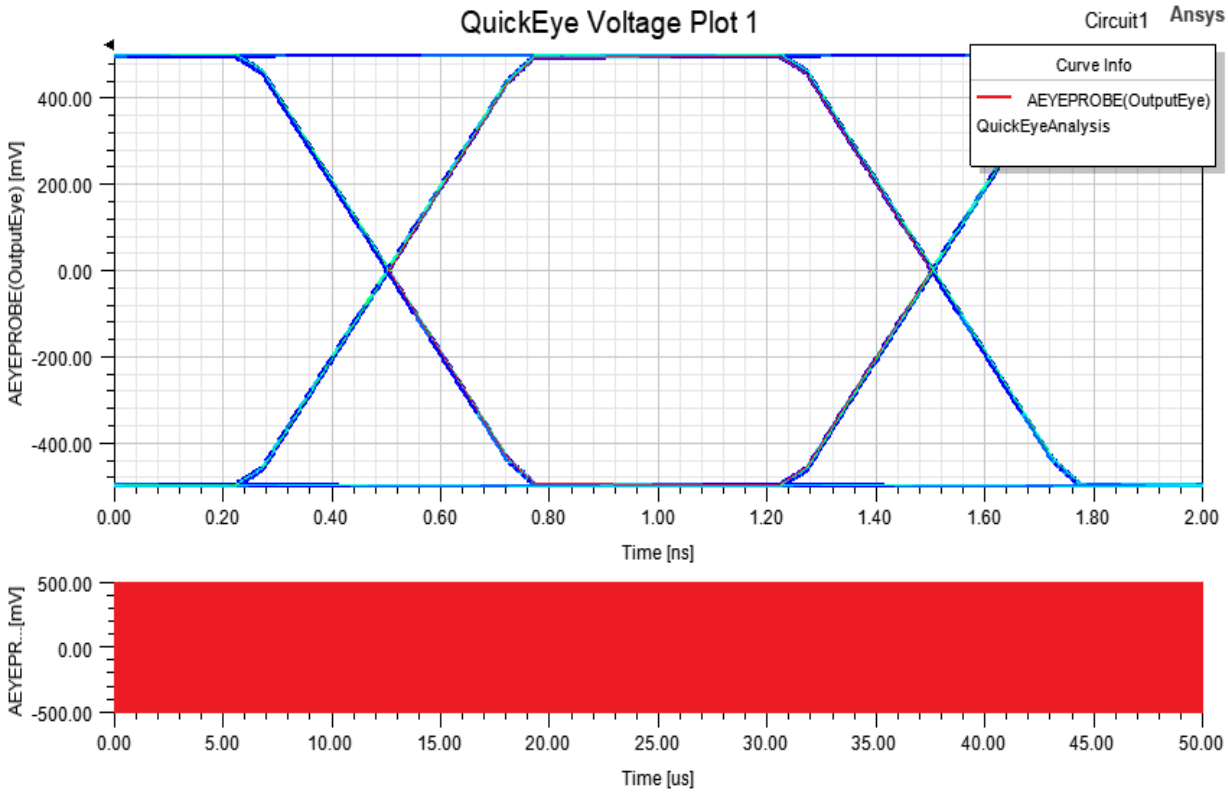
1. If necessary, on the **Project Manager** window, expand the **Project Tree** and [*active design folder*]. Then right-click the **Results** folder and select **Create Eye Diagram**

Report > **Rectangular Plot** to open the **Report** window.



2. From the **Context** group box, ensure that the **Solution** selection is **QuickEyeAnalysis**, the **Domain** selection is **Time**, and the Plotting Range values calculated by the solver are **Time Start: 0**, **Time Stop: 49.99995**. These are the default settings.
3. From the **Trace** tab, ensure that the **Primary Sweep** selection is **Time**, the **Category** selection is **Voltage**, the **Quantity** selection is **AEYEPROBE(OutputEye)**, and **<none>** is the **Function** selection. These are the default settings.
4. From the **Eye Parameters** group box, ensure that the **Unit Interval** is **"1e-009"**.

5. Click **New Report** to open the **"QuickEye Voltage Plot 1"** in the **View** tab. The graph shows the bit error rates calculated by QuickEye as an eye diagram.



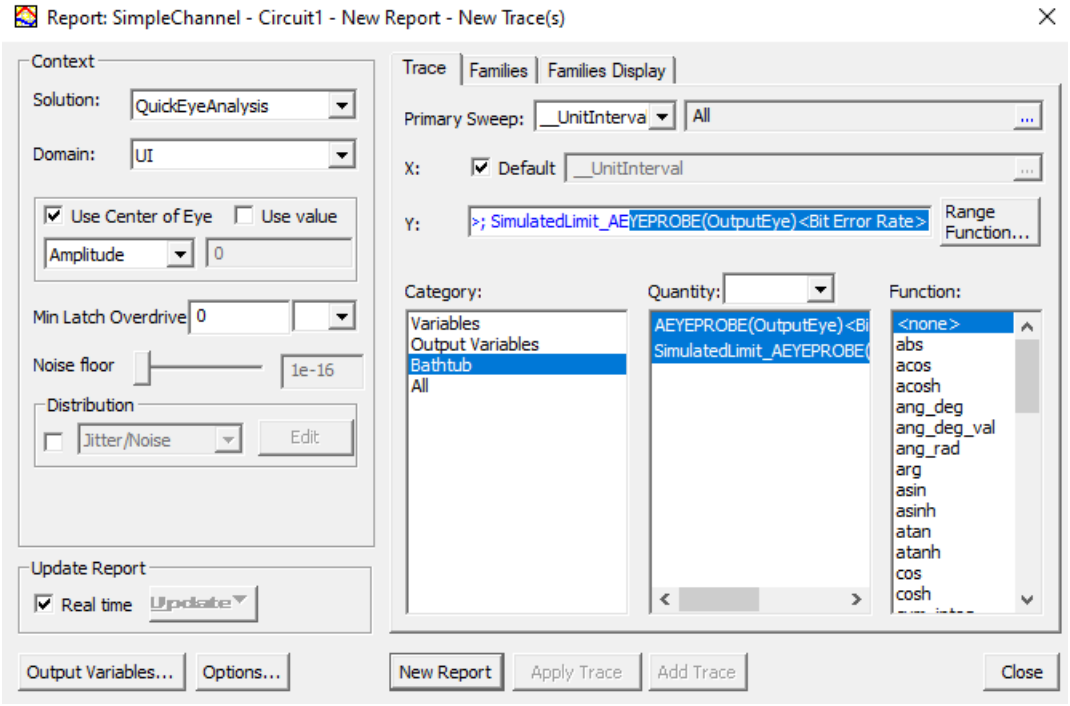
6. Click **Close** to close the **Report** window.

> **Note:** The Eye Source specifies transmit parameters such as jitter and equalization. For more information, see Channel Example with Gaussian Random Transmit Jitter.

Display a Bathtub Plot of the Quick Eye Analysis

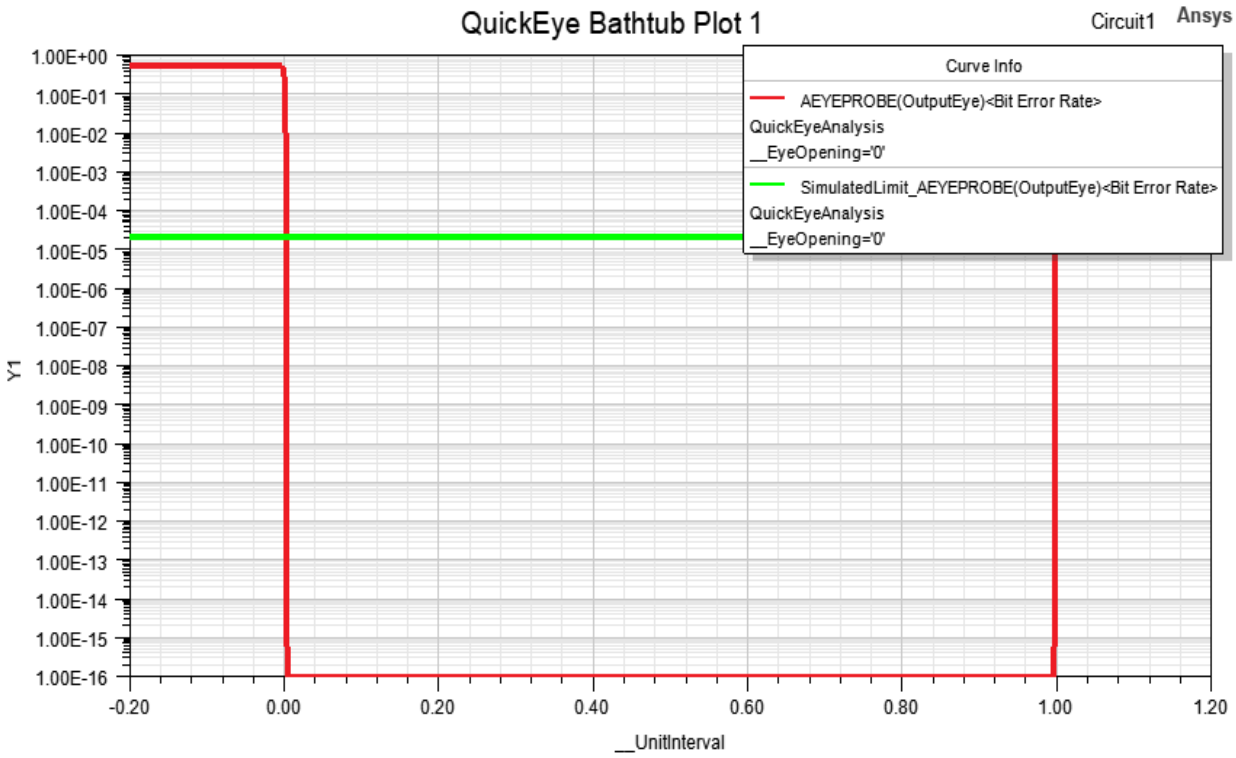
Complete the following steps to display a bathtub plot of the Quick Eye analysis.

1. If necessary, on the **Project Manager** window, expand the **Project Tree** and [*active design folder*]. Then right-click the **Results** folder and select **Create Standard Report** > **Rectangular Plot** to open the **Report** window.



2. From the **Context** group box, select **QuickEyeAnalysis** on the **Solution** drop-down menu.
3. Ensure the **Domain** selection is **UI**. This is the default setting.
3. From the **Trace** tab, ensure that the **Quantity** selection is **AEYEPROBE(OutputEye)** and **SimulatedLimit_AEYEPROBE(OutputEye)** by **Shift** + clicking to highlight both choices.
4. Ensure that the **Primary Sweep** selection is **_UnitInterval**, the **Category** selection is **Bathtub**, and **<none>** is the **Function** selection. These are the default settings.
5. Click **New Report** to open the **"QuickEye Bathtub Plot 1"** in the **View** tab. The graph shows the bit error rates calculated by VerifEye over the Unit Interval, together with the

limiting line.



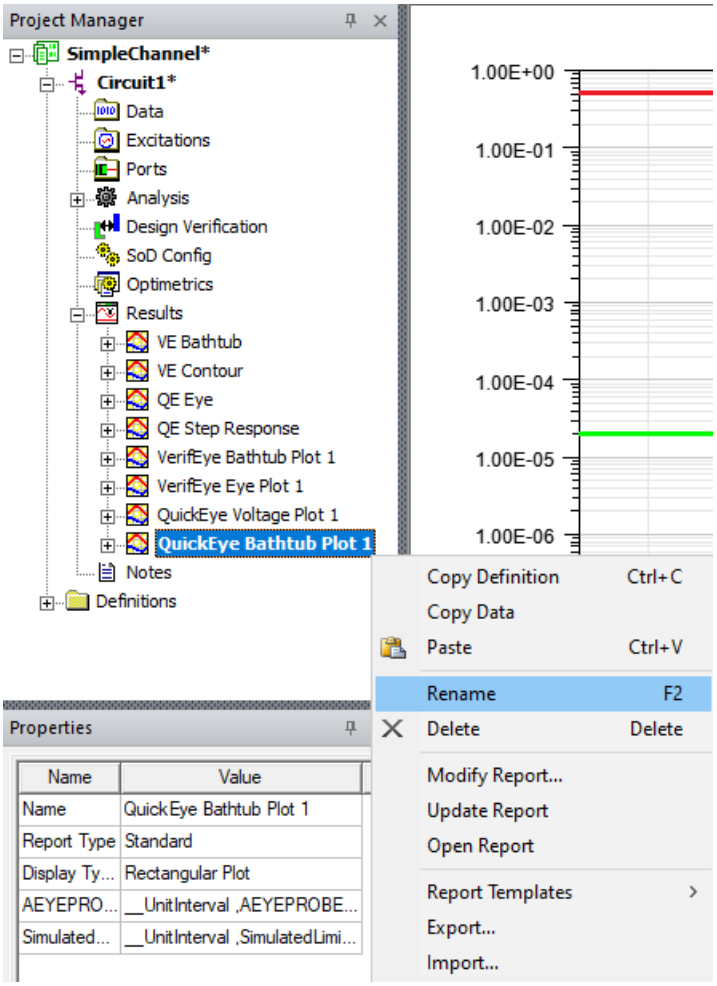
6. Click **Close** to close the **Report** window.

> **Note:** For bathtub curves of QE, distinguish simulated and extrapolated regions with a partitioning horizontal line using the 'SimulatedLimit' option that is in the 'Quantity' column (e.g., BER/SER level of partitioning = 1/bit or symbol_length simulated; symbol_length = bit_length for NRZ, or 0.5*bit_length for PAM4)

Rename a Report

To rename a report, on the **Project Manager** window, expand **Project Tree** > [*active design folder*] > **Results**. Then right-click the pertinent report icon (e.g., **"QuickEye Bathtub Plot 1"**) and select **Rename**. Type a new name into the field. When you are done, it will also appear over

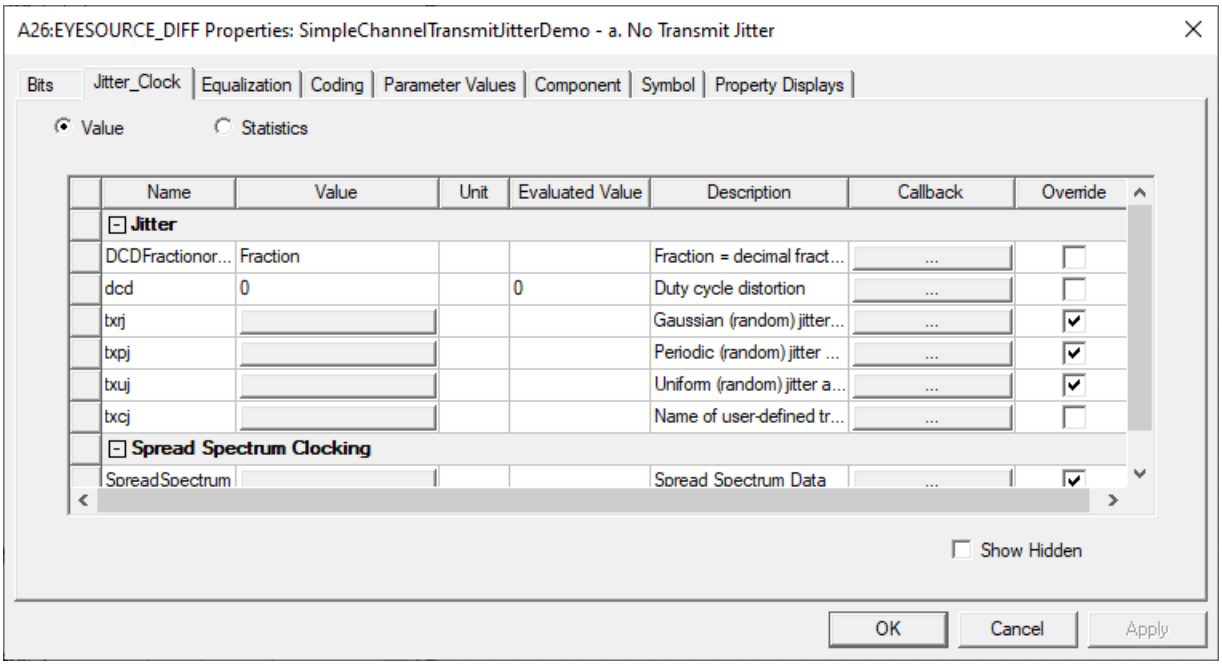
the plot in the **View** tab.



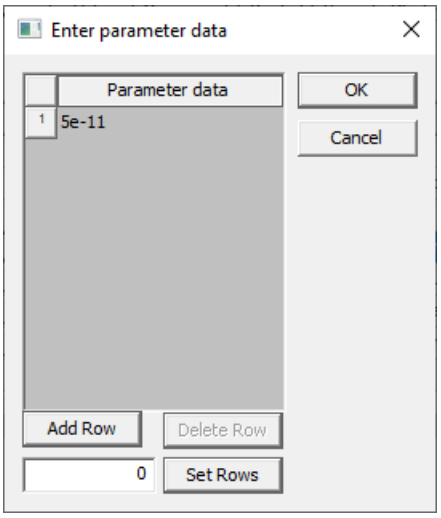
Add Transmit Jitter and Save the Project

Complete the following steps to add random Gaussian transmit jitter to the input signal, then save the project to preserve the analyses.

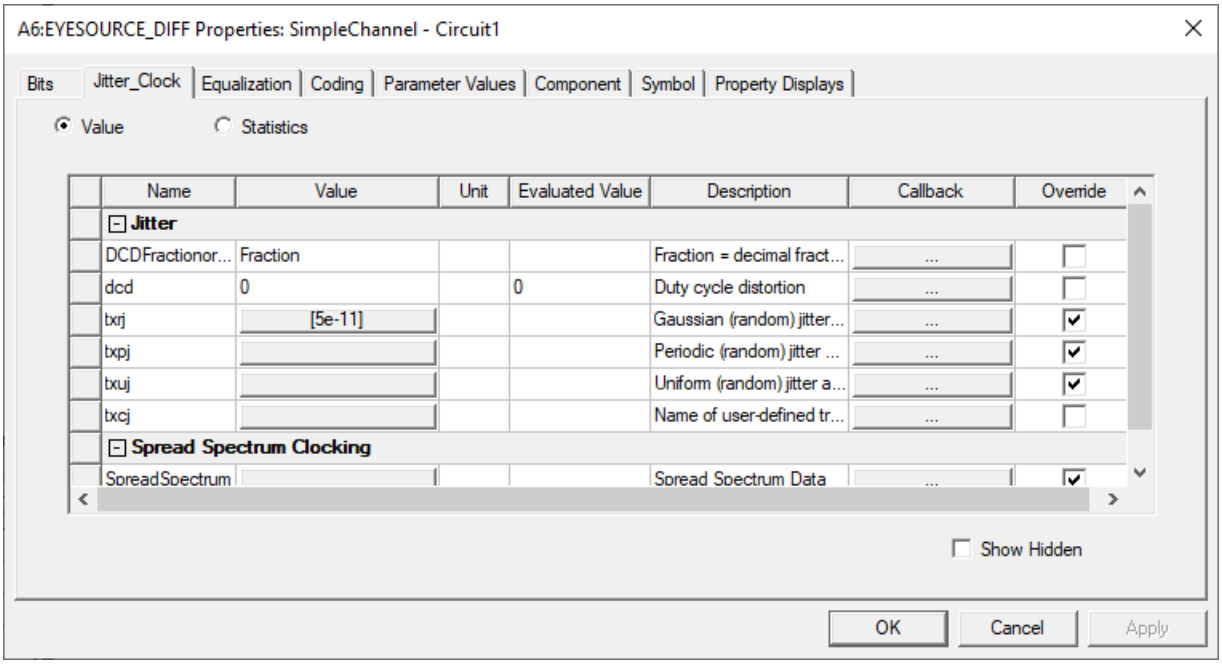
1. If necessary, return to the **Schematic Editor** by double-clicking [*active design folder*] (on the **Project Manager** window, expand the **Project Tree** to see [*active design folder*]). From the **Schematic Editor**, right-click the Eye Source and select **Properties** to open the component's **Properties** window. Then select the **Jitter_Clock** tab.



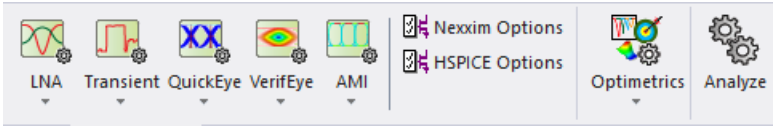
2. Click the **txrj Value Field** button to open the **Enter parameter data** window.



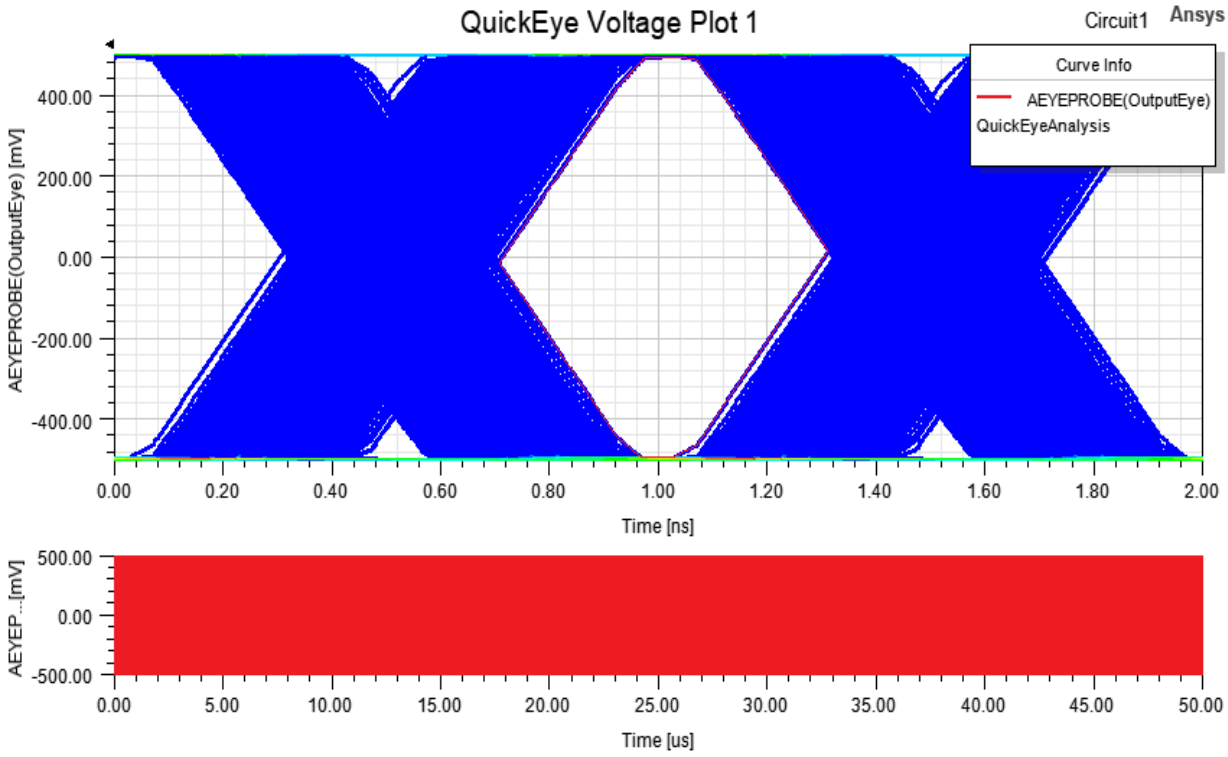
3. Enter **5e-11** in the invisible field next to the "1". 0.05ns is the standard deviation of the jitter distribution.
4. Click **OK** to close the **Enter parameter data** window.



3. Click **OK** to close the **Properties** window.
4. Select **Analyze** on the **Analysis** ribbon or, on the **Project Manager** window, expand the **Project Tree** and [*active design folder*] (on the **Project Manager** window, expand the **Project Tree** to see [*active design folder*]). Then right-click **Analysis**.

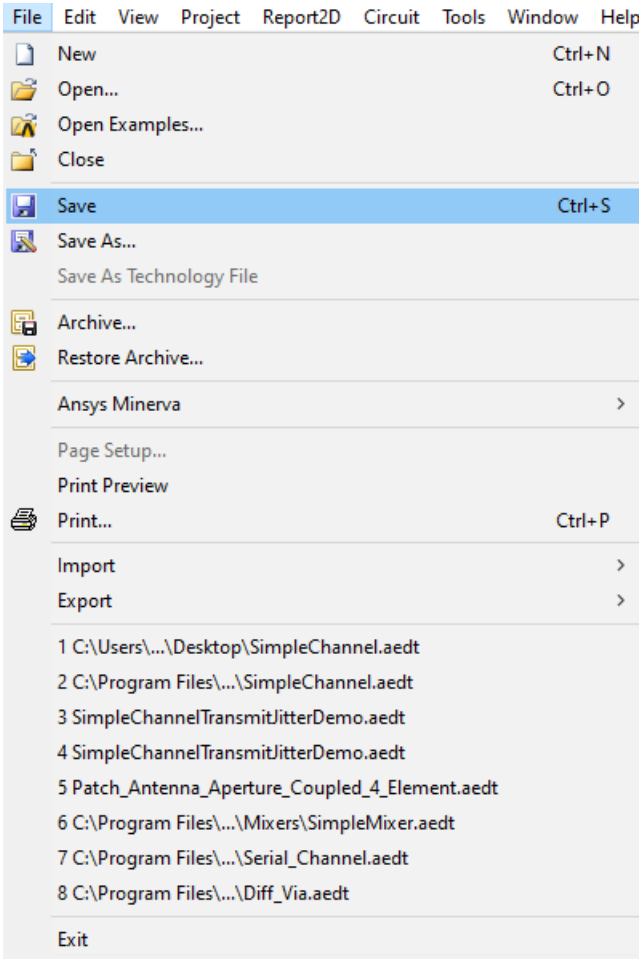


5. Click **Analyze** to rerun both simulations.
5. Open the VE and QE reports again to see the results with jitter.



Save the Project

When you are done, on the **File** menu, select **Save** to save the project.



The example procedures are complete.

Bathtub Plots/Curves

Bathtub plots are often seen in signal integrity analysis of high speed serial links(HSSL) and DDR systems. It shows BER performance with respect to sampling time (in UI) or voltage level, known as time or voltage bathtub curves respectively.

Bathtub curves are obtained based on QuickEye, VerifEye and AMI analyses in Nexxim. VerifyEye analysis uses statistical approach to compute bit error rate (e.g., symbol error rate for PAM4) from probability density function (PDF) of receiver voltage. It can provide reliable analytical BER/SER data down to 1e-14 region. Below that, numerical resolution in FFT/IFFT

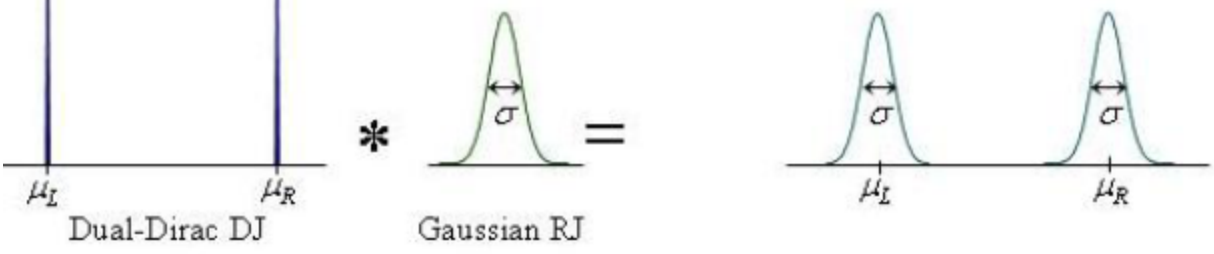
process makes results unreliable. QuickEye and AMI analyses, on the other hand, are all based on running a given number of random bits through the simulation system. Hence the simulated BER values are directly linked to number of bits simulated and can only go down to 1/number of bits simulated (for SER, 1/number of symbols simulated), typically in the range of 1e-5~1e-6 with reasonable time/space complexity. However, standards of high speed systems often demand eye opening measurements or jitter budgeting analysis at BER 1e-12 or lower. BER measurement down to 1e-12 region is beyond simulation reach.

Bathtub extrapolation predicts BER/SER performance using simulated or analytical data. Q-scale extrapolation is based on Dual-Dirac model for timing jitter noise, which is partitioned into deterministic jitter noise(DJ) and random jitter noise(RJ). DJ is bounded and modeled by sum of two Dirac Delta functions.

$$\mathrm{PDF}_{dual\text{-}Direc\ DJ}(x) = \delta(x - \mu_L) + \delta(x - \mu_R)$$

RJ is unbounded and follows Gaussian distribution N (0,♦ 2). Thus total jitter (TJ) follows.

$$[\delta(x-\mu_L)+\delta(x-\mu_R)] * \frac{1}{\sqrt{2\pi}\sigma}\exp\left(-\frac{x^2}{2\sigma^2}\right) = \frac{1}{\sqrt{2\pi}\sigma}\left[\exp\left(-\frac{(x-\mu_L)^2}{2\sigma^2}\right)+\exp\left(-\frac{(x-\mu_R)^2}{2\sigma^2}\right)\right]$$



Based on Dual-Dirac model, DJ impacts high BER region, while low BER region is only dependent upon tail of the RJ noise distribution. For more detail on Q-scale extrapolation, please refer to [4] and [5] in QuickEye, VerifEye and Bathtub Extrapolation References.

Due to the 'prediction' nature of extrapolation, certain amount of simulated data is needed for reasonably reliable extrapolation. Nexxim issues warning message when less than 250K random bits or 2^18 PRBS is set for QuickEye and AMI analyses when transmitter random jitter (txrj) is present. This lower limit of simulated bits assures simulated BER down to 1e-5 region is available for extrapolation with large enough txrj's for given sampling time resolution(in UI). It should be evident that the extrapolated part of the bathtub curves can benefit from more and reliable simulated data. Noisy and unreliable simulated BER's can adversely impact the quality of the extrapolated region.

VerifEye analysis does not rely on number of simulated bits. With typical txrj's, VE can provide bathtub curves down to 1e-14. Then extrapolation extends the curves to user selected noise floor as low as 1e-21 in Nexxim.